Electrical characterization and modeling of advanced SOI materials and devices

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Electrical characterization and modeling of advanced SOI materials and devices

Table of contents

List of acronyms **4**
List of constants **6**
List of symbols **7**
Chapter 1: General introduction **11**
1. Downscaling of MOSFETs 12
2. State-of-the-art 15
2.1 Starting substrate: SOI 15
2.2 Advanced architecture for three-dimensional SOI transistors 22
3. Objectives and organization of the thesis 26
Chapter 2: Characterization of heavily-doped SOI wafers by pseudo-MOSFET technique **39**
1. State-of-the-art for undoped SOI wafers 40
1.1 Experimental set-up for Ψ-MOSFET 41
1.2 Measurement configuration 42
1.3 Parameter extraction for undoped wafers 44
2. Experiments for heavily-doped (HD) SOI wafers 46
2.1 Sample preparation 46
2.2 Experimental results 47
2.3 Geometric factor for HD SOI wafers 50
2.4 Conventional Y-function for HD SOI wafers 52
3. Revisited model for HD SOI wafers 52
3.1 Variable volume contribution 53
3.2 Interface accumulation 56
3.3 Extracted results 58
4. Van der Pauw and Hall effect 60
4.1 Experiments set-up 60
4.2 Experimental results 62
4.3 Resistivity comparison 64
5. Conclusions and perspectives 65
Chapter 3: Characterization of metal bonded silicon wafers **70**
1. State-of-the-art for characterization of metal bonded wafers 71
2. Experiments set up 73

2.1 Sample preparation 73
2.2 Experimental configuration 74
2.3 Experimental results 75
3. TCAD simulation 78
3.1 Employed models 78
3.2 Simulation results 78
4. Model for estimation of bonded interface 81
4.1 Estimation principle 81
4.2 Experimental results 84
5. Conclusions and perspectives 86
Chapter 4: Parasitic bipolar effect in ultra-thin FD SOI MOSFETs 90
1. Contributions to drain leakage 91
1.1 Conventional drain leakage 92
1.2 Parasitic bipolar amplification 96
2. Evidence of parasitic bipolar effect in ultra-thin FD SOI MOSFETs 98
2.1 Experimental results 98
2.2 Simulations 101
3. Impact of back-gate on PBT 108
3.1 Experimental results 108
3.2 Physical mechanism of suppression of the PBT 109
4. Extraction of current gain for parasitic bipolar transistor 113
4.1 Conventional extraction methods 113
4.2 Ratio of drain leakage current between short- and long-channel devices 114
4.3 New extraction method based on back-gate biasing 119
5. Conclusions and perspectives 123
Chapter 5: Coupling effects in three-dimensional SOI devices 130
Part A: Modeling of potentials and coupling effects in inversion-mode and junctionless SOI FinFETs
1. Coupling effects in inversion-mode vertical DG SOI FinFETs 132
1.1 Experiments 132
1.2 Analytical model 136
2. Coupling effects in junctionless SOI FinFET 144
2.1 TCAD simulations 144
2.2 Modeling of 2D potential distribution in full depletion mode 149

Part B: Modeling of junctionless SOI FinFETs for parameters extraction

2.3 Modeling of carrier profile in partial depletion mode 157

2.4 Parameters extraction in accumulation mode 167

2.5 Conclusions on modeling of JL SOI FinFETs for parameters extraction 177

Part C: Application for parameters extraction in experimental GaN junctionless FinFETs

2.6 Experimental results 178

3. Conclusions and perspectives 180

Chapter 6: General conclusions and perspectives **185**

Abstract/Résumé **189**

Publications

Résumé du travail de la thèse en français

Acknowledgements

List of acronyms

Acronym	Nomination
1D, 2D and 3D	One, two and three-dimensional
2DEG	Two-dimensional electron gas
BESOI	Bond-and-etch-back SOI
BOX	Buried oxide
BTBT	Band-to-band tunneling
DIBL	Drain-induced barrier lowering
DWB	Direct wafer bonding
ELTRAN	Epitaxial Layer Transfer Wafer
EOT	Effective oxide thickness
ET	Extremely thin
ESFI	Epitaxial silicon films on insulators
FET	Field effect transistor
FinFETs	Finger field effect transistors
GAA	Gate-all-around
GaN	Gallium nitride
GeOI	Germanium-on Insulator
HDD/LDD	Heavily/lightly-doped source or drain concentrations
HEMT	High electron mobility transistor
ICs	Integrated circuits
II	Impact ionization
IM	Inversion mode
ITRS	International Technology Roadmap for Semiconductors
JAM	Junctionless accumulation mode
JL	Junctionless
MEMS	Micro Electro Mechanical Systems
MOS	Metal-oxide-semiconductor
MOSFETs	Metal-oxide-semiconductor field effect transistors
MPU	Microprocessor unit
MSD	Meta-Stable Dip
MuGFETs	Multiple gate field effect transistors
PBT	Parasitic bipolar transistor
RT	Room temperature
SAM	Scanning Acoustic Microscopy
SCEs	Short-channel effects
SEM	Scanning Electron Microscopy
SHE	Self-heating effect
SIMOX	Separation by Implantation of Oxygen
SIMS	Secondary ion mass spectrometry
SOS	Silicon-On-Sapphire

Acronym	**Nomination**
SRAM	Static Random-Access Memory
SS	Subthreshold swing
TCAD	Technology computer aid design
TEM	Transmission Electron Microscopy
TFET	Tunneling field effect transistor
TSV	Through Silicon Via
UTB	Ultra-thin body
UTBB	Ultra-thin body and buried oxide
WKB	Wentzel-Kramers-Brillouin
Ψ-MOSFET	Pseudo-MOSFET

List of constants

Symbol	Value/Unit	Description
A^*	32 $A/cm^2 \cdot K^2$	Effective Richardson constant for electrons
E_G	1.12 eV	Band gap for silicon
q	1.602×10^{-19} C	Electron charge
k	1.38×10^{-23} J/K	Boltzmann constant
ε_0	8.85×10^{-12} F/m	Vacuum permittivity
ε_{si}	$11.8 \times \varepsilon_0$ F/m	Silicon permittivity
ε_{GaN}	$12.9 \times \varepsilon_0$ F/m	Gallium nitride permittivity
ε_{Al2O3}	$9.1 \times \varepsilon_0$ F/m	Alumina permittivity
ε_{ox}	$3.9 \times \varepsilon_0$ F/m	Silicon dioxide permittivity

List of symbols

Symbol	Unit	Description
A		
A_{eff}	cm^{-2}	Effective area for Schottky diode
B		
B	T	Magnetic flux density
C		
C_{BOX}	F	BOX capacitance per unit area
C_{fin}	F	"Lateral" channel capacitance per unit area
C_{GC}	F	Capacitance between gate and channel per unit area
C_P	F	Parasitic capacitances coupling to the channel per unit area
C_{lox}	F	Capacitance for the oxide of side-gate per unit area
C_{tox}	F	Capacitance for the oxide of top-gate per unit area
E		
E_C	eV	Bottom edge of conduction band
E_F	eV	Semiconductor Fermi level
E_{FM}	eV	Metal Fermi level
$E_{F,n}$	eV	Quasi-Fermi level for electrons
E_{Fi}	eV	Intrinsic Fermi level
$E_{F,p}$	eV	Quasi-Fermi level for holes
E_V	eV	Top edge of conduction band
F		
f_G	unitless	Geometry factor for pseudo-MOSFET
G		
G_{BTBT}	$cm^{-3} \cdot s^{-1}$	Net generation rate for BTBT
g_m	S	Transconductance
I		
I_{acc}	A	Accumulation current
I_B	A	Base current
I_{bare}	A	Current for bare Si wafer
I_{bonded}	A	Current for bonded Si wafer
I_{BTBT}	A	BTBT current
I_C	A	Collector current
I_D	A	Drain current
I_{D_BG}	A	Drain leakage for short-channel devices with V_{BG} biased at a value negative enough to neutralize bipolar transistor
I_E	A	Emitter current
$I_{e,h\ BTBT}$	A	Electron/hole part of BTBT current
$I_{e\ C}$	A	Electron part of collector
$I_{e,hdiff}$	A	Electron or holes diffusion current
$I_{e,h\ II}$	A	Electron/hole part of impact ionization current
I_G	A	Gate current

Symbol	Unit	Description
I_{GC}, I_{GS} and I_{GD}	A	Gate-to-channel, gate-to-source and gate-to-drain current
I_{II}	A	Impact ionization current
$I_{intercept}$	A	Intercept current of I_D-W_{fin} curve
I_{MOS}	A	Intrinsic MOS current
I_{ON}	A	On-state current
I_{OFF}	A	Off-state current
I_P	A	Probe current
I_{PBT}	A	Parasitic bipolar transistor current
I_S	A	Source current
I_{Sat}	A	Reversed saturation current for Schottky diode
I_{sub}	A	Subthreshold conduction current
I_{vol}	A	Volume current
ΔI_D	A	Difference of drain current
J		
J_{e,h_iii} and $J_{e,h\ i}$	$A \cdot cm^{-2}$	Electron/hole current density in the horizontal direction
L		
L_G	nm	Gate length
L_p	nm	Size of square probe in the simulations
N		
n	unitless	Ideality factor of Schottky diode
n_{sub}	unitless	Subthreshold slope factor
N^*	cm^{-3}	Carrier density in the channel
$N_{A,D}$	cm^{-3}	Doping concentration for acceptors or donors.
N_{film}	cm^{-3}	Doping concentration of the film
N_{FD}	cm^{-3}	Criterion of carrier density at G-point enabling full depletion
n_i	cm^{-3}	Intrinsic carrier density
N_{LDD}	cm^{-3}	Doping concentration of LDD
R		
r	μm	Radius of tungsten probe for Jandel Universal Probe Station
R_{acc}	Ω	Access resistance
R_C	Ω	Contact resistance
R_{C1}	Ω	Resistance at Probe/Silicon interfaces
R_{C2}	Ω	Resistance at Silicon/Chuck interfaces
R_{eff}	Ω	Effective resistance at the bonding interface
r_H	unitless	Hall scattering factor
R_H	m^3/C	Hall coefficient
R_{input}	Ω	Series resistance for metal-bonded wafers
R_{TiN}, R_{Ti}, R_{Si}	Ω	Parasitic resistance for TiN, Ti and silicon
$R_{\square}$	Ω	Sheet resistance
S		
SS	mV/dec	Subthreshold swing
T		

Symbol	Unit	Description
T	K	Temperature
T_{BOX}	nm	Thickness of BOX
T_p	nm	Penetration depth of probe
T_{si}	nm	Thickness of silicon film
T_{FD}	nm	Maximum body thickness for single-gate junctionless
T_1	nm	$W_0 ar\tanh\eta_1$
T_2	nm	$W_0 ar\tanh\eta_2$
V		
V_{BG}	V	Back-gate voltage
V_C	V	Chuck voltage
V_D	V	Drain voltage
V_{FB}	V	Flat-band voltage
V_{FBF}/V_{FBB}	V	Flat band voltage for front/back-channel
V_{FG}	V	Front-gate voltage
V_G	V	Gate voltage
V_H	V	Hall voltage
V_{MT}	V	Measured voltages of top layers in Kevin cross
V_{MB}	V	Measured voltages of bottom layers in Kevin cross
V_P	V	Probe voltage
V_S	V	Source voltage
V_T	V	Threshold voltage
V_{THF}/V_{THB}	V	Threshold voltages of front/back-channel
ΔV_{FG}	V	Shift of front-gate voltage from minimum drain leakage
W		
W	nm	Width of channel
W_0	nm	Width of channel
W_D	nm	Width of depletion layer
W_{Dmax}	nm	Maximum width of the depletion region
W_{fin}	nm	Width of the fin
W_{FD}	nm	Maximum body width for double-gate junctionless
X		
x	nm	Axis in the horizontal direction
Y		
y	nm	Axis in the vertical direction
Y	$A^{0.5}V^{0.5}$	Conventional Y-function
Y_{acc}	$A^{0.5}V^{0.5}$	Adapted Y-function for accumulation layer
α_n	nm	Average distance for avalanche generation
β	unitless	Bipolar gain
$\varphi_{acc}/\varphi_{inv}$	V	Surface potential for an accumulation/ inversion layer
φ_F	V	Fermi potential
φ_m	V	Maximum surface potential of back-gate
φ_s	V	Surface potential
φ_{sb}	V	Surface potential of back-gate
φ_{sl}	V	Surface potential of lateral-gates
φ_{sf}	V	Surface potential of top-gate

Symbol	Unit	Description
φ_T	V	Band bending with respect to Fermi level
ϕ_B	V	Barrier height of Schottky diode
$\varphi(x)$	V	Electrostatic potential in the Si film
$\Phi_{S,M}$	V	Work-functions for silicon or metal
χ	eV	Electron affinity energy
η_{PBT}	unitless	Ratio of drain currents (PBT efficiency)
λ	unitless	Front coupling effect coefficient
μ_0	cm^{-2}/Vs	Low-field mobility
μ_{acc}	cm^{-2}/Vs	Mobility for accumulation layer
μ_H	cm^{-2}/Vs	Hall mobility
μ_p	cm^{-2}/Vs	Hole mobility
μ_n	cm^{-2}/Vs	Electron mobility
μ_s	cm^{-2}/Vs	Interface mobility at Si/BOX interface
μ_{vol}	cm^{-2}/Vs	Volume mobility
ξ	unitless	Back coupling effect coefficient
θ_{acc}	V^{-1}	Degradation factor of mobility
ρ	$\Omega \cdot cm$	Resistivity
ρ_{VDP}	$\Omega \cdot cm$	Average resistivity from Van der Pauw experiments

Chapter 1: General introduction

1. Downscaling of MOSFETs

Since Lilienfeld patented the basic concept of the field effect transistor (FET) in 1930 [1] and J. Kilby realized the first integrated circuits (ICs) in 1958 [2], the semiconductor manufacturers have been sparing no efforts to fabricate advanced microelectronic components with lower power, faster speed and higher integration. This strategy is strongly supported by the technology downscaling of planar bulk silicon-based metal-oxide-semiconductor field effect transistor (MOSFET), well-known as "Moore's law" [3]. Figure 1.1 shows the scaling trend of the microprocessor unit (MPU) projected by ITRS 2011. It shows that the physical gate length follows a 3.8-year cycle trend beginning from 2009 (29 nm node). In 2016, the physical gate length will reach 16 nm.

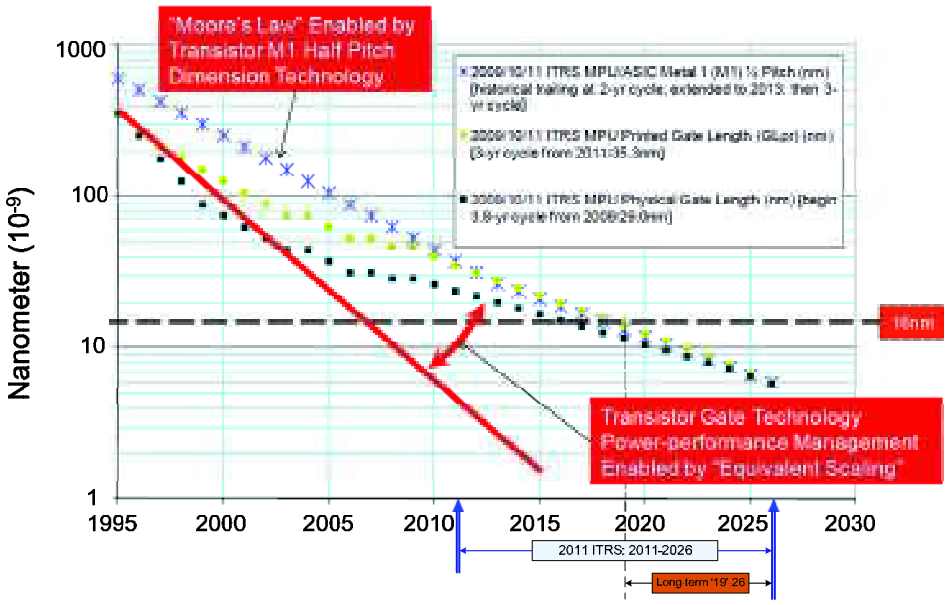

Figure 1.1: *Scaling trend projected by ITRS 2011 [4].*

However, the conventional planar bulk MOSFET is approaching the physical limits of scaling:

— With the gate oxide (T_{si}) decreasing, the gate leakage increases exponentially [5]. In order to reduce the gate leakage, hafnium-based high-k gate stacks have successfully been introduced as gate insulator [6], [7], as shown in Figure 1.2.

For further scaling such as sub-20 nm, new generation of high-k materials is demanded to obtain thinner Equivalent Oxide Thickness (EOT) [8], [9].

— With the gate length (L_G) shrinking, the lateral electric fields at the source and drain penetrate into the channel and reduce barrier height of source/body junction in the OFF-state. This will enhance the carrier injection and the OFF-state current, leading to unnegligible power consumption. In order to continue "Moore's law", new structures with better electrostatic control are employed, such as multiple gates or ultra-thin body (UTB) silicon-on-insulator (SOI) devices [10].

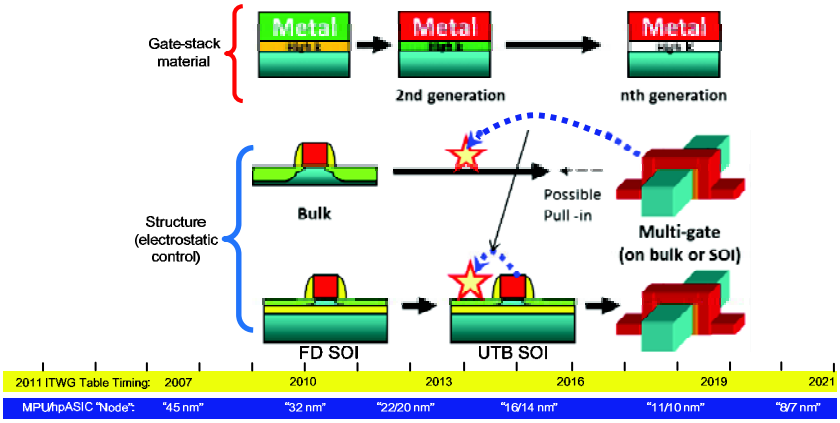

Figure 1.2: *New technologies for further scaling including high-k/metal gate stack, FDSOI and multi-gate structures (adapted from [4]).*

Jacobson summarized most silicon technologies competing for further scaling and gave the benchmark based on the comparison of ON-state current (I_{ON}) and OFF-state current (I_{OFF}), as shown in Figure 1.3 [11]. The best performance devices are at the right bottom corner and exhibit higher I_{ON}/I_{OFF}. Unfortunately, no device structure locates at that corner:

— The junctionless accumulation mode (JAM) device [12] has the minimum I_{OFF} (~ 10^{-13} A), but it exhibits a low I_{ON} (~ 10^{-5} A).

— Tunneling FET (TFET) [13] has a small I_{OFF} (~ 10^{-9} A), but it also has a low I_{ON} (~ 6 × 10^{-5} A).

— The ultra-thin body SOI (UTB) [14], multiple gate (Tri-gate) [15], [16], impact ionization (IMOS) [17] and metal source/drain (MSD) [18] devices suffer from high I_{OFF} (~ 10^{-7} A), but all of them provide high I_{ON} (~ 10^{-3} A).

Considering the performance demanded by ITRS (I_{ON} ~ 10^{-3} A) [4], the semiconductor manufacturers mainly focus on UTB and multiple gate devices in sub-30 nm nodes. With the help of thin body, 28 nm FD SOI devices have been achieved in STMicroelectronics [14], [19] and IBM [20], [21]. On the other hand, Intel has successfully applied the tri-gate technology to its 22 nm processors [22]. These devices are currently being optimized for 14 nm node. For further sub-20 nm technology, the SOI FinFET is a more appropriate solution due to its low power and high performance [23]. In addition, the junctionless accumulation mode transistors with a heavily-doped channel show compelling advantages in suppression of short-channel effects (SCEs) [24], [25], albeit they suffer from random doping fluctuations.

In this thesis, we mainly dedicate to the electrical characterization and modeling of advanced silicon materials and SOI devices for ultimate micro-nano-electronics. In next section, we will introduce the advantages and challenges of SOI technology.

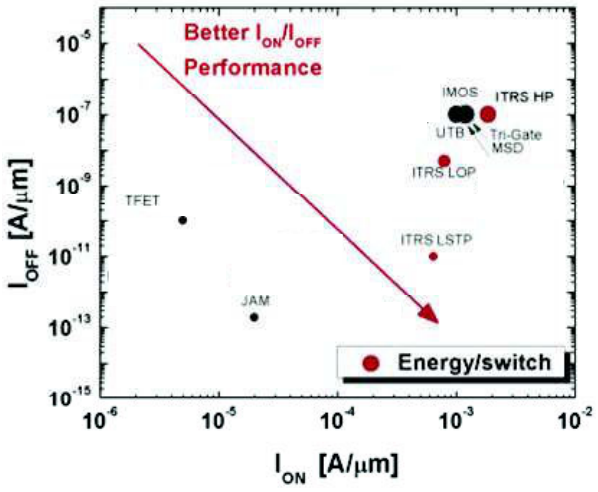

Figure 1.3: *Benchmarking normalized ON- and OFF-state currents [11]. Devices with small bubbles have lower energy per switching event. Red dots indicate ITRS targets.*

2. State-of-the-art

2.1 Starting substrate: SOI

The SOI technology originates from the research on Silicon-On-Sapphire (SOS) in 1960-1970s [26], which was only applied in spaceborne and military electronics due to high cost. In 1978, K. Izumi from NTT in Japan successfully implanted oxygen below devices to form an insulating layer [27]. Since then, many methods to fabricate SOI substrates have been developed such as Separation by Implantation of Oxygen (SIMOX) [28], [29], Bond-and-Etch-Back SOI (BESOI) [30], [31], Epitaxial Layer Transfer Wafer (ELTRAN) [32] and Recrystallization of Polysilicon [33]. However, it was not until the late 1990s that a milestone fabrication process named Smart-Cut^{TM} was invented by Michel Bruel from CEA-Leti [34]. His extraordinary concept promoted the widespread application of SOI substrates in semiconductor industrials.

The SOI substrate comprises three layers: the active silicon film device layer, the buried oxide (BOX) and the silicon substrate, as shown in Figure 1.4. Transistors are integrated in the active silicon film, while the substrate serves for mechanical support [33]. Depending on the thickness of silicon film, the SOI substrates can be divided into two groups, partially-depleted (PD) and fully-depleted (FD) SOI [35], [36]:

- **PD SOI substrates** correspond to film thickness $T_{si} > 2W_{Dmax}$, (W_{Dmax} denotes the maximum width of the depletion region). Therefore, a neutral region subsists in the film when the transistor works in weak and strong inversion (Figure 1.4a).
- **FD SOI substrates** correspond to film thickness $T_{si} < 2W_{Dmax}$. This leads to the overlap of the depletion zones induced at the front-gate and back-gate interfaces. Thus, the interface potentials interact by coupling [37], as shown in Figure 1.4b.

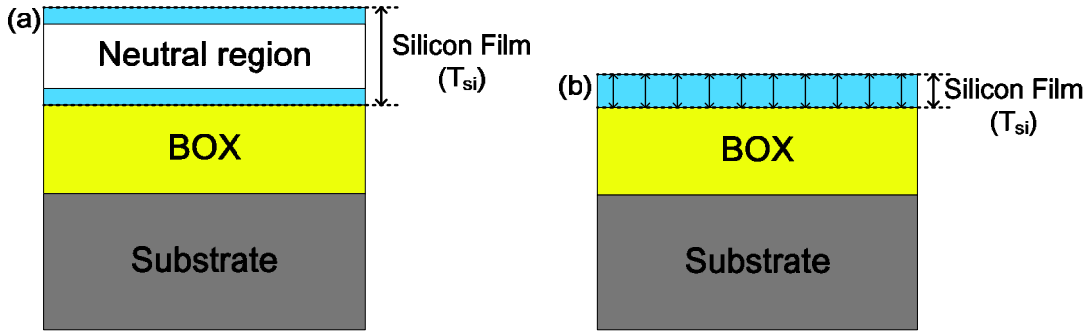

Figure 1.4: *Schematic of the (a) PD and (b) FD SOI structure.*

2.1.1 Advantages of SOI CMOS technology

- **PD SOI CMOS technology**

Compared with bulk silicon transistors, PD SOI technology has several advantages [38]–[42]:

— The buried oxide simplifies the isolation of devices, and completely avoids the parasitic effects such as latch-up, charge sharing and leakage between devices [39], [40].

— Due to the natural isolation by the oxide, SOI devices are immunized from radiation effects (especially single-event effects due to charge in the channel) [38].

— SOI circuits exhibits less parasitic capacitance, substrate noise and energy consumption due to lower leakage and supply voltage [41], [42].

- **FD SOI technology**

For further scaling, the ultra-thin FD SOI MOSFETs have been arousing special interest [14], [43]–[46]. Compared with PD SOI, they have additional key advantages:

— **Reduction of short-channel effects (SCEs):** Benefiting from the ultra-thin body, the leakage paths between source and drain triggered by SCEs are suppressed, leading to limited the threshold voltage (V_T) roll-off and finally to the reduction of OFF-state current and power (Figure 1.5a) [36], [47], [48]. On

the other hand, drain-induced barrier lowering (DIBL) can also be reduced with the film thickness shrinking, as shown in Figure 1.5b [49]. Thinner BOX also leads to smaller DIBL due to the reduction of fringing field through the BOX and substrate [50]. In addition, the ideal subthreshold swing (~ 60 mV/dec) is achieved in ultra-thin FD MOSFETs [19].

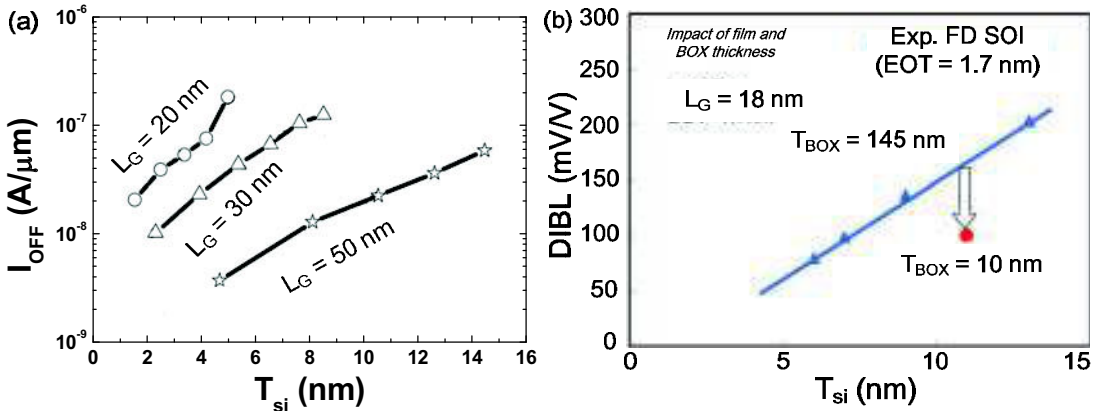

Figure 1.5: *(a) OFF-state current versus film thickness for SOI [48] and (b) impact of film and BOX thickness on DIBL [49].*

— **Multiple threshold voltage:** Another attractive feature for FD SOI devices is the back-gate, which enables to adjust the threshold voltage (V_T) for low power management [51], [52] (Figure 1.6). Compared with bulk silicon technology, where threshold voltage can only be tuned by process such as channel implanting and gate work function engineering, tuning V_T by back-gate in FD technology is much simpler and more flexible. Wise back-gate bias also helps improving the carrier mobility [53] and SCEs [54].

— **Undoped channel:** An undoped channel, typical for ultra-thin FD MOSFETs, avoids the mobility degradation from channel doping and reduces the variability of the threshold voltage induced by dopants fluctuation [55]–[57].

Although ultra-thin FD SOI technology shows unrivalled advantages in suppressing short-channel effects (SCEs) and exhibits high performance, it still faces some issues, which will be explained in section 2.1.2.

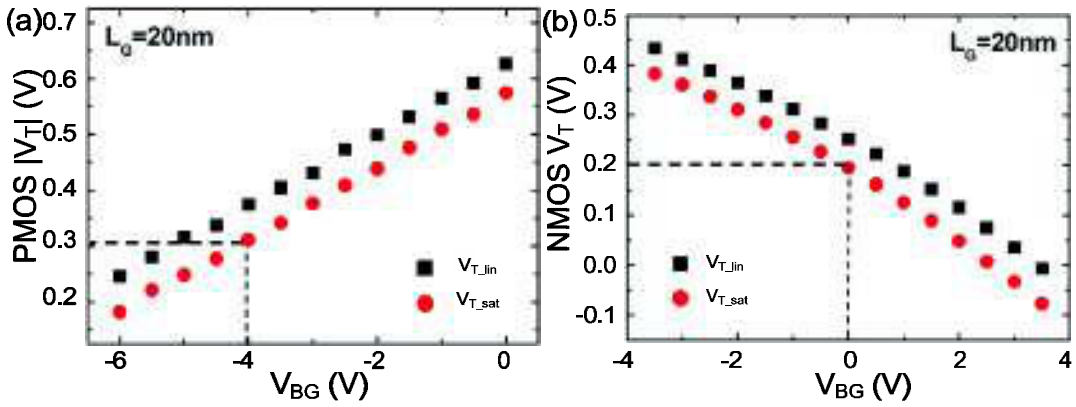

Figure 1.6: *Coupling between front-channel threshold voltage V_T and back-gate bias showing impact of film and BOX thickness: (a) PMOS and (b) NMOS [52].*

2.1.2 Challenges of FD SOI technology

Despite compelling advantages for sub-30 nm node due to good control of electrostatic potential in the channel, FD SOI MOSFETs suffer from: increase of parasitic source/drain resistance [58]; diffusion of source/drain dopants [59]; readiness of ultra-thin SOI wafers [60], [61]; self-heating effect [62]–[65]; parasitic bipolar effect [66], [67]; coupling effects [68], [69]. In this thesis, we focus on the parasitic bipolar and coupling effects.

- **Parasitic bipolar effect**

As mentioned previously in PD SOI technology, the depletion zones do not overlap and the electric potentials of the two interfaces (gate oxide/Si film and Si film/BOX) remain independent, leading to a 'floating' body at the bottom of the channel [70], [71]. This floating body can trigger kink effect and parasitic bipolar action in PD SOI devices [72]. For FD SOI MOSFETs, the kink effect almost disappears (impossibility to collect majority carrier in the body that would affect the threshold voltage), but the parasitic bipolar effect still happens as long as the drain voltage is high enough [73]. Recently, Fenouillet-Beranger *et al.* noted a parasitic bipolar effect in ultra-thin FD SOI MOSFETS (T_{si} = 10 nm) [74]. The parasitic bipolar can be triggered either by impact ionization (II) [66], [75] or by the band-to-band tunneling (BTBT) [76] around

the drain region. This parasitic bipolar effect can enhance the drain leakage, as discussed in chapter 4.

The floating-body effect is not always detrimental:

— Based on the transient floating-body effect, a capacitor-less single SOI transistor memory was developed [77].
— Using the BTBT, coupling and floating-body effect, Bawedin *et al.* proposed the Meta-Stable Dip memory cell [78].
— The Z-RAM cell was developed utilizing the parasitic bipolar effect induced by impact ionization [79].

- **Coupling effects**

The coupling effects between front- and back-gates happen when the thin SOI film is fully depleted [80], [81]. For thick body, the neutral region cuts off the link between front and back channels (Figure 1.4a). However, No such neutral region exists in ultra-thin FD SOI (Figure 1.4b), leading to interactions between front- and back-channels. The coupling effect affects the threshold voltage and mobility in the channel.

An additional coupling originates from the BOX/substrate interface. Substrate depletion is regarded as a key limiting factor, such as enhancement of DIBL, threshold voltage roll-off and parasitic back-channel conduction [82], [83]. A heavily-doped layer under the BOX, called ground plane, is adopted to suppress the substrate depletion effect [14].

Besides the PD and FD SOI substrates, there are other innovative substrates for advanced MOSFETs, which will be introduced in section 2.1.3.

2.1.3 Innovative materials for advanced MOSFETs

The development of the film layer transfer technology allows the conception of

transistors with innovative materials, such as strained silicon [84]–[86] and Germanium-on-Insulator [87], [88], III-V materials [89], SiC [90], GaN on insulator [91]. Here, we focus on ultra-thin heavily-doped SOI wafers, three-dimensional integration and III-V compound materials.

- **Ultra-thin heavily-doped SOI wafers**

Heavily-doped silicon layers are needed for the source/drain engineering of MOSFETs [92] and junctionless transistors (see section 2.2.2) [12], [93]. The formation of heavily-doped and ultra-thin silicon layers involves several questions: activation of dopants; implant uniformity and defects induced at the Film/BOX interface [20], [94], [95].

Another application of heavily-doped silicon layer is the tuning of threshold voltage [96], [97]. In advanced MOSFETs, mid-gap metal gate is often used to avoid the depletion of conventional polycrystalline silicon gate [98], [99]. Thus, the doping of the channel becomes the only solution left to tune the threshold voltage. Akarvardar *et al.* have successfully used the fin doping to adjust the threshold voltage in SOI FinFETs [100].

- **Three-dimensional integration**

Historically, the memory access time has improved less than 10% per year, though processor has shown 60% performance improvement per year. In fact, this “memory wall” is more pronounced in the popular multicore chips. Besides, the wire delay caused by interconnects is exacerbated when billions of transistors are integrated in one chip. All these issues can be solved by the 3D integration, which is a promising technology in “Beyond More” era. It dates back to the 1970s and 1980s when a variety of digital, power and optical devices has been prototyped [101]. Early application of 3D integration can also be seen in Dynamic Random Access Memory for higher packing density [102], [103]. The 3D integration can improve

interconnection based on Through Silicon Vias, enabling more than 100,000 vias per square centimeter [104]. More attractively, 3D integration allows dissimilar materials, process technologies and functionalities to be co-integrated. According to the size of integrated units, 3D integration can be achieved by chip-to-chip, chip-to-wafer and wafer-to-wafer bonding. Figure 1.7 shows the schematic structures of two super chips with multiple functionalities, respectively achieved by multichip-to-wafer and wafer-to-wafer bonding technique. Compared with the two other methods, wafer-to-wafer bonding provides an ultimate solution for manufacturing due to low cost and simple process.

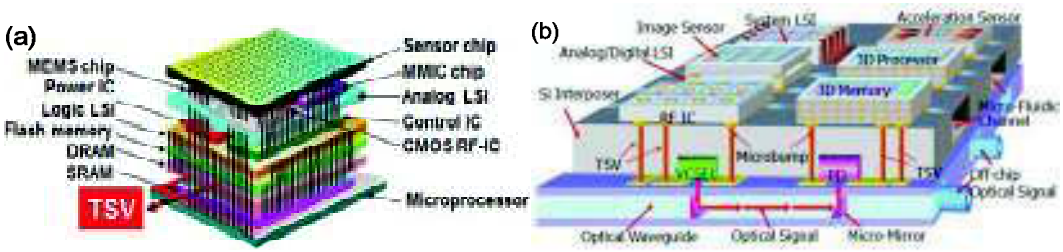

Figure 1.7: *Schematic structure for two 3D chips with multiple functionalities by: (a) chip-to-wafer and (b) wafer-to-wafer [105].*

The wafer-to-wafer bonding can be categorized into direct bonds, anodic bonds, and bonds with intermediate layers [106]. In all wafer-to-wafer technologies, direct wafer bonding has shown a more compelling advantage in terms of bonding quality and mechanical attachment, alignment capability, reliability and cost. For example, the directly-bonded wafers exhibit sufficient high-temperature stability, thus permitting a wide range of subsequent processes.

- **III-V compounds on Insulator**

Compared with silicon, III-V compounds are widely used to fabricate high electron mobility transistor (HEMT) due to faster mobility, larger breakdown voltage and higher temperature tolerance [89]. For HEMT, the 2D conductive channel is formed by a heterojunction. More attractively, a layer of two-dimensional electron gas (2DEG)

would be generated at the interface between undoped (GaAs in this example) and n-doped III-V (AlGaAs) [11]. This 2DEG effect can be attributed to diffusion of electrons from the n-doped wide bandgap region into the undoped material. The 2DEG devices experience reduced scattering and increased mobility. However, HEMTs have shown difficulties in forming a high-quality gate dielectric on these materials and in controlling the high gate leakage due to Schottky source/drain [107].

Besides GaAs, Gallium Nitride (GaN) is also an appealing channel material for MOSFETs [108]. The 2DEG is formed at AlGaN/GaN interfaces [109]. However, the GaN-based devices still face challenges, including high drive current at low voltage, decreased gate leakage, integrated p-type transistors and enhancement mode devices [110], [111].

2.2 Advanced architecture for three-dimensional SOI transistors

Different from planar transistors, 3D devices have multiple gates: vertical double-gate [112], triple-gate [113] and quadruple-gate [114]; FinFETs can be either vertical double-gate or triple-gate structures. The wrap-around gate structure provides the best electrostatic control over the channel and thus helps in reducing the leakage current and short-channel effects [115]. According to their operating mechanism, the 3D transistors can be divided into inversion-mode and accumulation mode.

2.2.1 Inversion-mode MOSFETs

Since Intel corporation successfully fabricated its “Ivy Bridge” processors based on 22 nm triple-gate technology in 2012 [113], triple-gate transistors have been a hot spot for the unprecedented combination of excellent performance and energy efficiency. These transistors utilize a single gate wrapped around the channel, as shown in Figure 1.8a. This allows for essentially three times increased surface area for electrons or holes to transport. Similar to conventional planar MOSFETs, inversion-mode triple-gate device is turned on when the inversion layer is triggered in

the channel. In bulk triple-gate technology, halo implantation and channel doping are required to achieve shallow source/drain junction and tune the threshold voltage, which increases the variability caused by dopants [100].

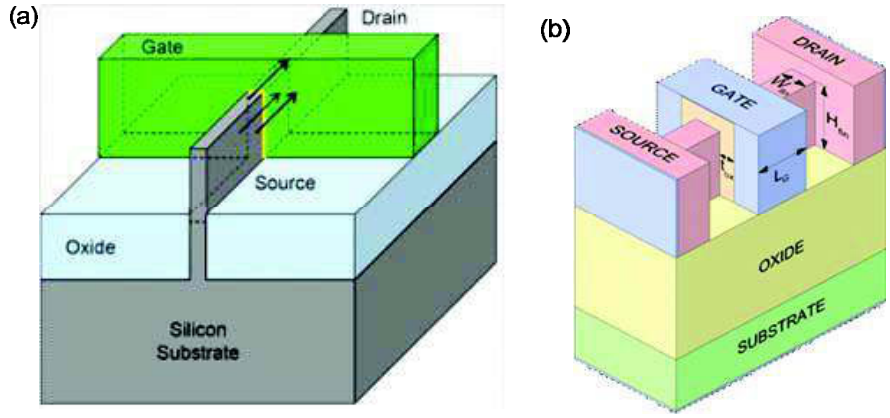

Figure 1.8: *Schematic of a bulk triple-gate transistor and a SOI FinFET* ***[115]****.*

On the other hand, FinFETs fabricated on SOI substrates have great potential in sub-20 nm nodes (Figure 1.8b), since they can inherit the advantages from both FD SOI and FinFET [10]. Researchers from GlobalFoundries and IBM corporations have demonstrated 14 nm multi-fin SOI FinFETs [116]. Even SOI FinFET with 10 nm gate length has been achieved [117], [118]. Compared with bulk FinFET, SOI FinFETs exhibit many compelling advantages [10], [115], [119], [120]:

— Shallower junction depth (lower junction capacitance) due to the natural barrier (BOX) against dopants diffusion;
— No punch-through due to the thin film and BOX;
— Higher mobility and reduced threshold voltage mismatch due to low-doped channel;
— Better control of SCEs;
— Easier mobility boosters such as strained SOI and Si/Ge.

However, 3D structures still face some challenges:

— For further scaling, more advanced photolithography is needed to fabricate narrower fins.
— The enhanced quantum confinement in extremely narrow fin can cause

mobility degradation [117].

— The coupling effect between the multiple gates is amplified in narrow FinFETs [69].

— The corner effect amplifies the local electric field, so optimized design is demanded, such as Ω-FinFET [121].

2.2.2 Accumulation-mode and junctionless MOSFETs

Junctionless transistor is a variant of accumulation-mode MOSFETs proposed by J. P. Colinge based on gate-controlled heavily-doped nanowires (10^{19} cm^{-3} for n-type and 10^{18} cm^{-3} for p-type) [93]. Different from the traditional inversion-mode transistor (n-p-n for n-type MOSFET or p-n-p for p-type MOSFET), the transistor without junctions behaves like a resistor in ON-state. The OFF-state is achieved by the complete depletion of carriers in the film, where the resistance of the channel becomes quasi-infinite. Figure 1.9 shows the schematic of the working mechanisms for junctionless transistors.

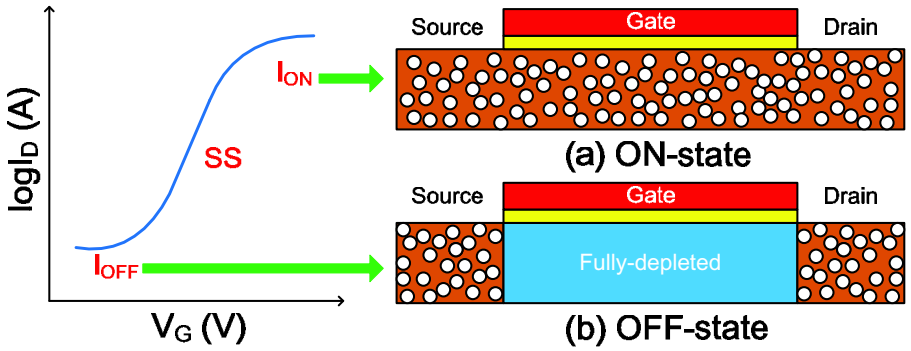

Figure 1.9: *Schematic of working mechanisms for junctionless transistors: (a) ON-state and (b) OFF-state.*

Junctionless transistors have attracted attention for nano-channel applications:

— Simplified source/drain junction engineering which permits controlling the SCEs such as DIBL due to the absence of diffusion of source and drain impurities into the channel region [122]. Basically, the channel length is

defined by the gate, not by the source/drain implants.

— To ensure full depletion, the film thickness or the nanowire cross-section should be extremely small (< 5-10 nm). Benefited from this small cross-section, the junctionless transistors exhibit low DIBL and subthreshold slope (SS), as shown in Figure 1.10a. It was claimed that with L_G scaling down to 10 nm, the performance of junctionless transistors is better than inversion-mode transistors [123], but this topic is controversial.

— The roll-off of threshold voltage is apparently suppressed in junctionless transistors (Figure 1.10b) [123].

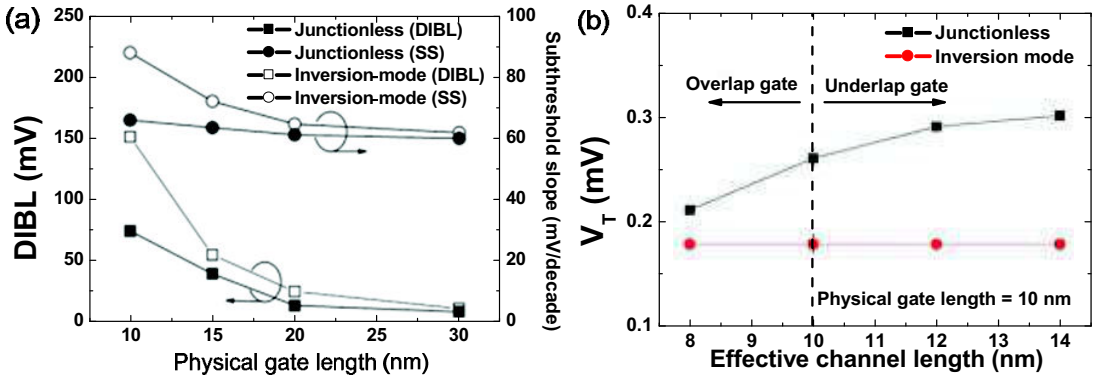

Figure 1.10: (a) Comparison of DIBL and SS between junctionless and inversion mode transistors for different gate lengths; (b) threshold voltage of junctionless and inversion mode devices as a function of effective channel length at V_D = 50 mV [123].

However, there are serious trade-offs to be considered in the design of junctionless transistors:

— The mobility can benefit from the reduced vertical electric field in high doped channel, but it is obviously degraded due to increased doping level [122]. Mobility enhancement techniques are employed to increase the ON-state current [124].

— No over implanting of source/drain leads to better control of SCEs, but to higher parasitic resistance. Therefore, higher doping level is used for source and drain (compared to the channel) to reduce the access resistance [125]. In this case, the device is no longer junstionless and falls into the category of accumulation-mode

MOSFETs with heavy channel doping.

— Very high doping is responsible for random doping fluctuations that cause the threshold voltage variability issues [126].

— The inter-gate coupling is strong in the subtheshold region, but vanishes in ON-state [127].

3 Objectives and organization of the thesis

In this thesis, we aim at the electrical characterization and modeling in advanced silicon materials and SOI devices. The thesis contains five more chapters and is organized as follows:

— In chapter 2, we investigate the characterization of heavily-doped SOI materials under pseudo-MOSFET, Hall effect and four-point probe configurations. These materials were dedicated to junctionless transistors, which aroused other interest in advanced CMOS devices (FD SOI and 3D FinFETs).

— Chapter 3 will discuss how to characterize and model the metal-bonded wafers by using current-voltage measurements in view of interconnect optimization for 3D circuits.

— In chapter 4, we focus on the parasitic bipolar effect, which affects the OFF-region in ultra-thin FD SOI MOSFET. The physical mechanisms of parasitic bipolar effect in short-channel FD SOI devices will be revealed from experiments and simulations. Two methods are proposed to extract the bipolar gain.

— Chapter 5 is dedicated to multiple gate transistors. We systematically investigate the coupling effect in both inversion-mode and junctionless SOI FinFETs. 2D analytical models are proposed: one gives the potential distribution and the other gives the carrier profile. We also show how to extract parameters in nano-channel junctionless devices and discuss the limits

of validity of the methods.

— Chapter 6 will give the conclusions of this thesis and perspectives for future work.

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Chapter 2: Characterization of heavily-doped SOI wafers by pseudo-MOSFET technique

Heavily-doped (HD) silicon-on-insulator (SOI) wafers have been a promising solution in several respects: source/drain engineering [1], [2], junctionless transistors [3], [4], multiple threshold voltage tuning [5], *etc.* For all these applications, it is critical to measure the doping activation, carrier mobility and implantation-induced defects.

In this chapter, we develop a characterization method for the transport properties of HD SOI under pseudo-MOSFET configuration. An adapted model for parameter extraction will be developed. Additional Hall effect and four-point probes experiments are carried out for validation of our extraction method.

1. State-of-the-art for undoped SOI wafers

Pseudo-MOSFET (also called Ψ-MOSFET) is one of the most efficient methods for characterization of SOI films [6]. It has been widely used as a quick and accurate technique for monitoring as-fabricated SOI wafers because it does not require any CMOS processing [7]–[9]. In the Ψ-MOSFET method, the silicon film represents the body of the transistor and the buried oxide serves as the gate insulator. If the substrate is biased as a gate, inversion or accumulation layers will be induced at the Film/BOX interface. Depending on the contacts used as source and drain, two main versions of test configuration exist:

— **Point-contact Ψ-MOSFET:** Two metal probes with controlled pressure are used as source and drain, as shown in Figure 2.1a. This technique was developed by Cristoloveanu *et al.* in 1992 at IMEP [6]. The metallic pressure probes allow ohmic contact, so both electrons and holes can be collected [6]–[9].

— **Hg-FET:** Two mercury circles are deposed on the surface of SOI wafers as source and drain, as shown in Figure 2.1b. This technique was firstly proposed by Hovel in 1996 at IBM [10]. The geometry (channel length and width) for Hg-FET is clearly defined [10], [11]. However, this technique suffers from the effect of parasitic resistance caused by the Hg/Si contact.

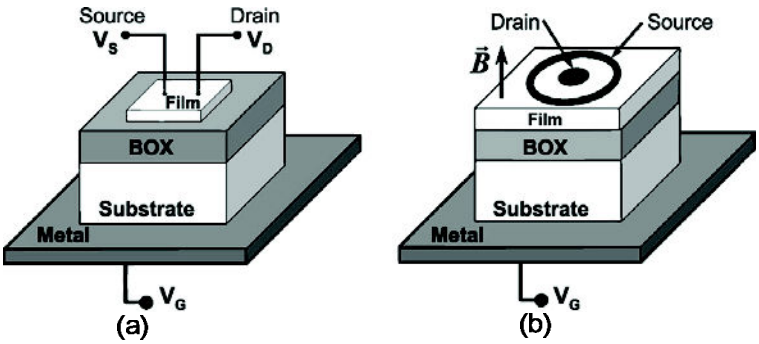

Figure 2.1: *Schematic configuration for: (a) point-contact Ψ-MOSFET and (b) Hg-FET.*

Since the Ψ-MOSFET works like an upside down MOSFET, standard parameter-extraction methods from MOSFETs can be employed to determine the material parameters (threshold and flat-band voltages, mobility of electrons and holes, interface traps, oxide charges, *etc.*) [5], [7]–[9]. Due to its simplicity and efficiency, the point-contact Ψ-MOSFET (Figure 2.1a) with pressure probes is intensely used for the characterization of undoped SOI films. Before adapting it to our doped samples, we will firstly describe it in details in the next sub-section.

1.1 Experimental set-up for Ψ-MOSFET

The experiments of point-contact Ψ-MOSFET are performed using a standard Jandel Universal Probe Station, as shown in Figure 2.2. It contains a copper chuck and 4 tungsten carbide probes with a tunable pressure (0 ~ 100 g) [12]. The tip radius of the probes is about 40 μm and the distance between two successive probes is of 1 mm. A hinged light shield can cover the entire measurement apparatus.

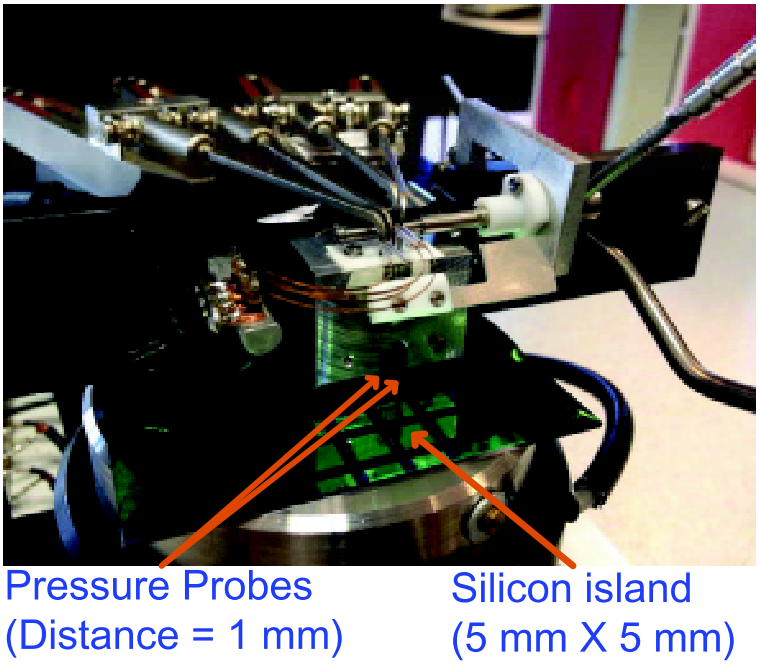

Figure 2.2: *Experimental platform for point-contact Ψ-MOSFET.*

1.2 Measurement configuration

Typically, silicon islands with square shape (5 × 5 mm^2) are etched on the wafer in order to avoid the effect of edge leakage, as shown in Figure 2.2. All the measurements are performed with an Agilent 4156B Semiconductor Analyzer at room temperature. In order to avoid the hysteresis effects [8], [13] and make sure that all the the measurements are done in steady state, some precautions are taken:

- **Hold time:** standby time before the beginning of a measurement is set as 5 s.
- **Delay time:** standby time between two successive gate biases equals to 0.02 s.
- **Integration time:** total measurement time for each point (i.e. each bias) of the $I(V)$ characteristic. The trade-off between reducing measurement errors caused by noise and limiting the measurement speed, leads to a choice of medium integration time (0.02 s).

Before the measurements, two problems must be solved:

- **Choice of the drain voltage**

Since the drain current increases linearly with the drain bias in ohmic region, this region is often employed to characterize the point-contact Ψ-MOSFET based on simple models [7], [14]. In order to identify the ohmic region, drain current-drain

voltage ($I_D(V_D)$) measurements must be performed. Figure 2.3 gives the $I_D(V_D)$ curve for undoped SOI wafers with 40 nm film thickness and 145 nm BOX thickness from SEMATEC. For both negative and positive gate bias, the drain current always increases linearly in the measured region (−0.4 V < V_D < +0.4 V). For our next studies, we will use a V_D of 0.2 V, which guarantees an ohmic functioning regime.

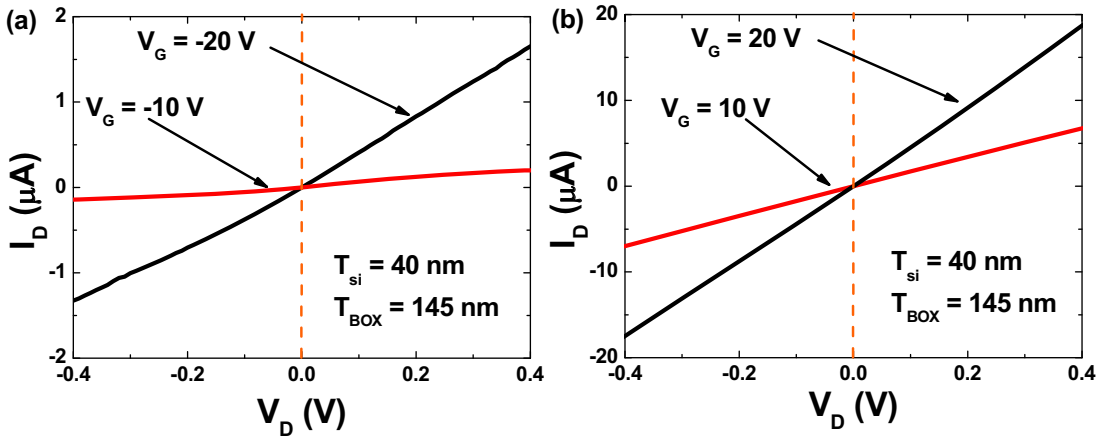

Figure 2.3: *$I_D(V_D)$ curves with (a) negative and (b) positive gate bias (V_G) for undoped SOI wafer under Ψ-MOSFET configuration. Probe pressure is 60 g.*

- **Choice of probe pressure**

The second consideration is the probe pressure. A metallic probe on low-doped (or undoped) silicon film is expected to result in a Schottky contact. From Figure 2.3, it is obviously that the contacts are ohmic and not Schottky (since the $I_D(V_D)$ curves are linear). According to [15], the contact between pressure probe and silicon becomes ohmic probably due to trap-assisted tunneling. However, detailed measurements by Ionica *et al.* [16] indicate that the connection from Schottky contact to ohmic contact results from the pressure-induced damage. With the probe pressure rising, for thick SOI wafers, the drain current increases, as shown in Figure 2.4a. Does the probe pressure affect the drain current similarly for thin films? Figure 2.4b shows that the drain current for 40 nm film thickness firstly increases (from 30 g to 60 g) and then saturates (60 g ~ 70 g). Here, we used 60 g for 40 nm SOI samples. The 10 nm samples shown later in this chapter were measured with 30 g only to avoid BOX leakage.

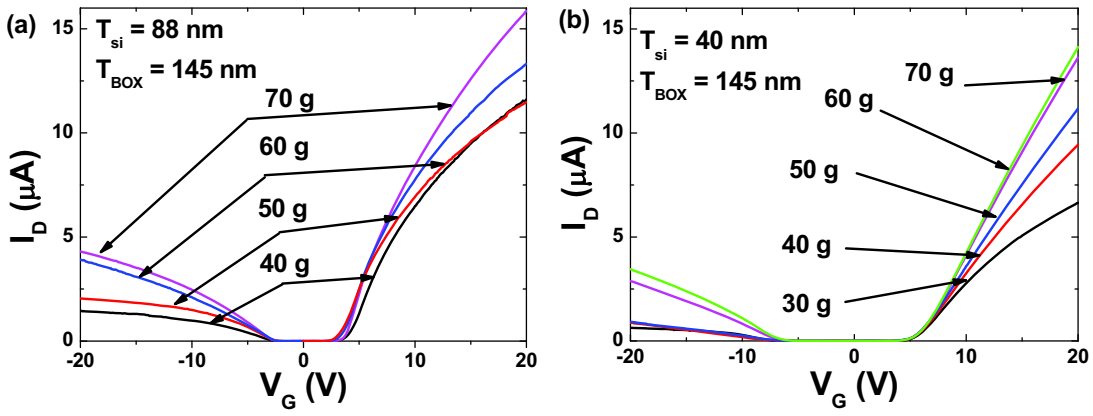

Figure 2.4: *$I_D(V_G)$ curves with different probe pressure under Ψ-MOSFET configuration for: (a) thick and (b) thin undoped wafers. V_D = 0.2 V.*

1.3 Parameter extraction for undoped wafers

Figure 2.4 shows that a drain current is visible for both $V_G < 0$ and $V_G > 0$ in undoped wafers [7]. When the gate bias is negative, the holes are accumulated near the Film/BOX interface (Figure 2.5a); if the gate voltage is positive, the electrons form an inversion layer at the Film/BOX interface (Figure 2.5b). Both electrons and holes can be characterized with Ψ-MOSFET in undoped SOI wafers. Figure 2.6a shows the typical $I_D(V_G)$ curve obtained in ohmic region with V_D = 0.2 V, while Figure 2.6b shows the corresponding transconductance g_m ($g_m = dI_D/dV_{FG}$).

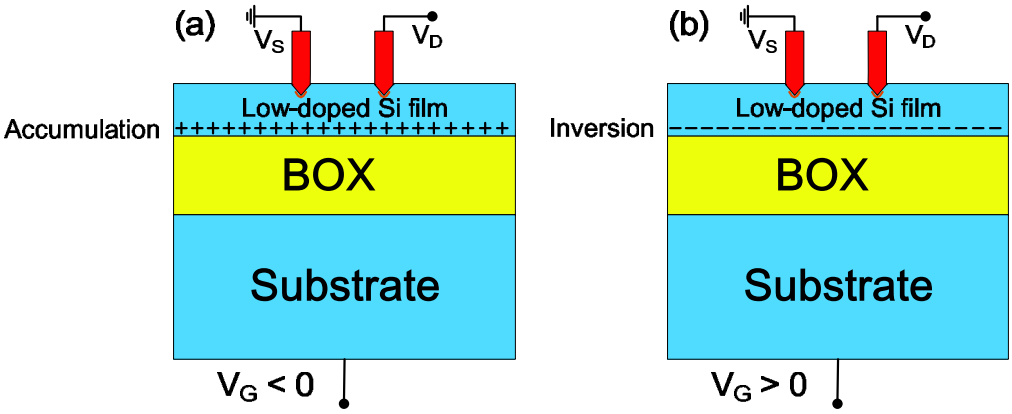

Figure 2.5: *(a) Accumulation channel and (b) inversion channel in Ψ-MOSFET for low-doped Si film.*

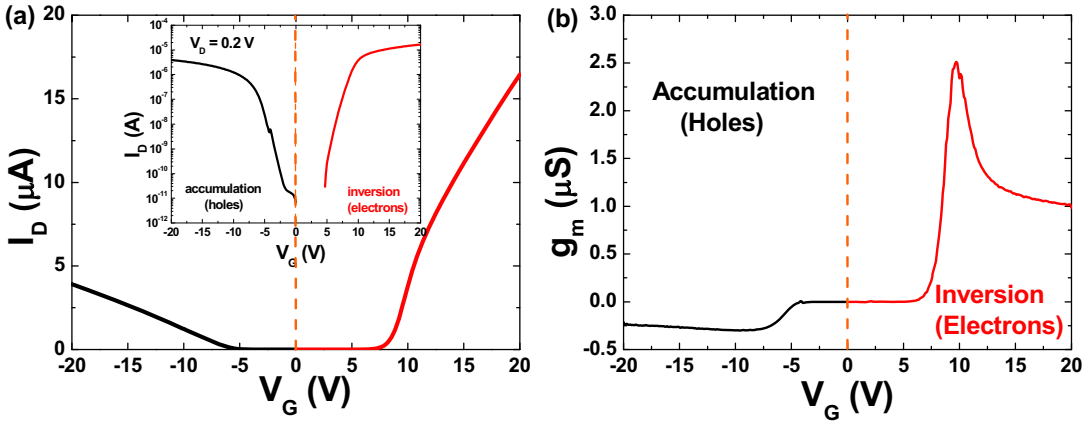

Figure 2.6: *Typical curves of drain current and transconductance in undoped thin SOI wafer: (a) $I_D(V_G)$ (inset: semi-logarithmic scale of $I_D(V_G)$) and (b) $g_m(V_G)$. T_{si} = 40 nm, T_{BOX} = 145 nm and V_D = 0.2 V. The probe pressure is 60 g.*

The drain current for a long-channel planar MOSFET in the linear region of operation can be modeled as [17]:

$$I_D = \frac{W}{L_G} C_{OX} \frac{\mu_0}{1+\theta(V_G - V_T)} (V_G - V_T) V_D \tag{2.1}$$

where W and L_G are respectivly the width and length of the channel, C_{OX} is the capacitance of gate oxide per unit area, μ_0 is the low-field mobility (μ_p for holes and μ_n for electrons), θ is the degradation coefficient of mobility and V_T represents the threshold voltage. Consequently, the corresponding transconductance in ohmic region can be written as:

$$g_m = \frac{dI_D}{dg_m} = \frac{W}{L_G} C_{OX} \frac{\mu_0}{\left[1+\theta(V_G - V_T)\right]^2} V_D \tag{2.2}$$

For Ψ-MOSFETs, W/L_G cannot directly be obtained. An empirical geometric factor f_G for point-contact Ψ-MOSFETs was calculated in [6], ~ 0.75 for undoped SOI wafers. With respect to the conventional MOSFETs, the Ψ-MOSFETs can also work in accumulation mode, as shown in Figure 2.6. In this case, V_T is replaced by the flat-band voltage V_{FB} in Eqs. (2.1) and (2.2) [7].

The Y-function is an efficient and simple method for parameters extraction of MOSFETs [18]. Combing Eqs. (2.1) and (2.2), the Y-function for Ψ-MOSFETs can be expressed as:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{f_G C_{BOX} V_D \mu_0}(V_G - V_{T,FB}) \tag{2.3}$$

The Y-function is linear with V_G for undoped wafers, as shown in Figure 2.7. The intercept of Y-function with V_G axis yields the threshold voltage V_T for inversion channel or the flat-band voltage V_{FB} for accumulation channel. The slope of the Y-function allows extracting the low-field mobility. The advantage of Y-function is that the series resistance and the reduction of low-field mobility with vertical electric field (both included in θ) are eliminated. For the undoped sample with T_{si} = 40 nm, the Y-function is plotted in Figure 2.7 and we obtained: V_{FB} = −6.1 V and μ_p = 94 cm^2/Vs for holes; V_T = 6.9 V and μ_n = 457 cm^2/Vs for electrons.

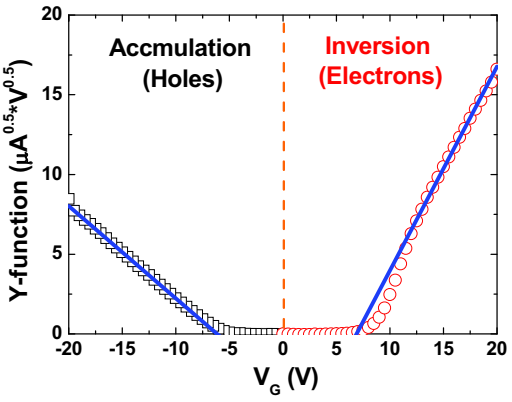

Figure 2.7: *Y-function versus gate voltage for undoped thin SOI wafer. T_{si} = 40 nm, T_{BOX} = 145 nm and V_D = 0.2 V.*

2. Experiments for heavily-doped (HD) SOI wafers

The Ψ-MOSFET is obviously a simple technique to extract electrical parameters of low-doped SOI films. Here we were interested in the possibility to use it for highly-doped SOI wafers.

2.1 Sample preparation

The SOI wafers from SEMATEC were characterized in view of several applications. Two types of Si films were compared in our measurements: 40 nm thick with ~10^{19} cm^{-3} target doping and 10 nm thick with ~10^{20} cm^{-3}. Wafers were implanted with three types of dopants (arsenic, phosphorus and boron) and annealed at 1070℃. Undoped SOI wafers with 40 nm thick film were also fabricated and used as a reference. The samples specifications are detailed in Table 2-I.

Table 2-I: *Description of SOI samples used in the experiments.*

SOI Samples	Implanted Dose (cm^{-2})	Film Thickness (nm)	BOX Thickness (nm)
SOI_ref (reference)	undoped	40	145
SOI_40	8×10^{13}	40	145
SOI_10	5×10^{15}	10	145

2.2 Experimental results

We performed the Ψ-MOSFET measurements for HD SOI wafers on the same experimental platform as for undoped SOI wafers (Figure 2.2). Before the $I_D(V_G)$ curves were tested under Ψ-MOSFET configuration, we determined the linear region. Figure 2.8 shows the $I_D(V_D)$ curves for HD SOI wafers. When V_D is swept from −3 V to +3 V, the drain current for all the three HD SOI wafers increases linearly under negative and positive gate bias. In order to compare with undoped wafers, we set V_D as 0.2 V for all the doped samples, as it was for the undoped wafers.

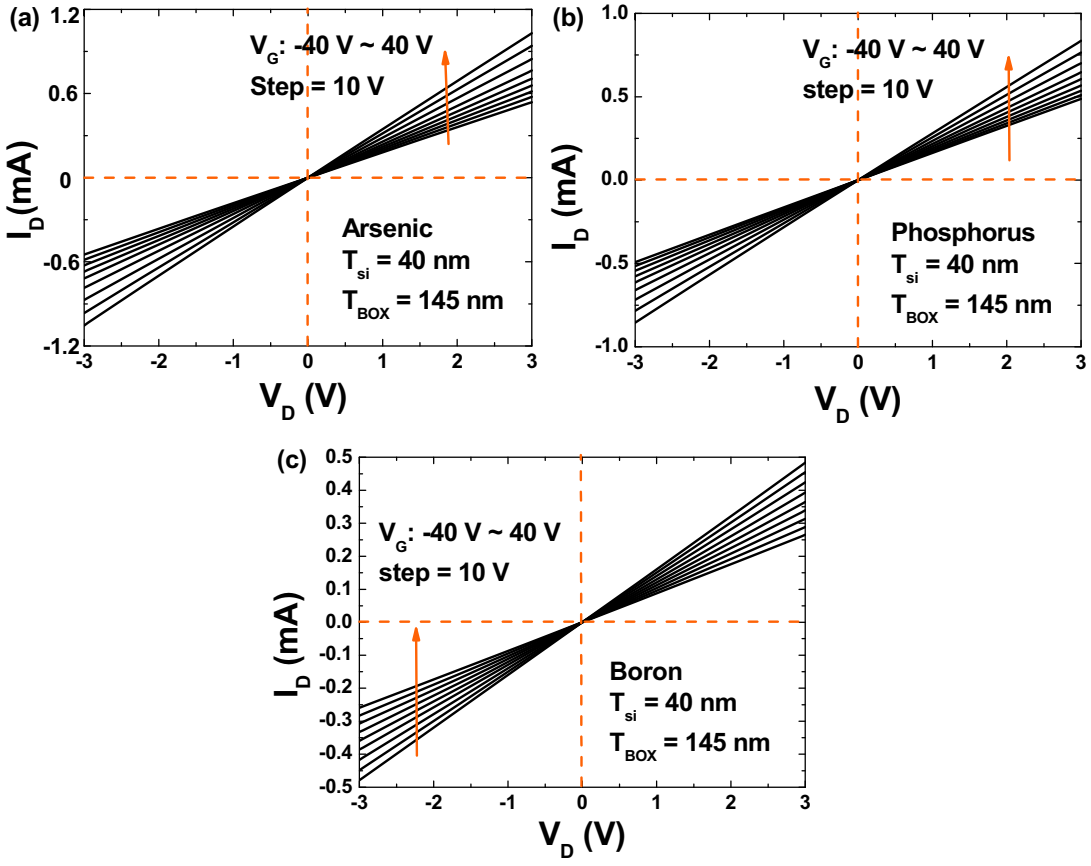

Figure 2.8: *$I_D(V_D)$ curves with different V_G bias under Ψ-MOSFET configuration for (a) arsenic-implanted, (b) phosphorus-implanted and (c) boron-implanted SOI wafers. Probe pressure is 60 g.*

Figure 2.9 shows the $I_D(V_G)$ and $g_m(V_G)$ curves for doped SOI wafers: (a) and (b) for n-type dopants (As and P); (c) and (d) for p-type (B). The $I_D(V_G)$ characteristics for 40 nm HD SOI wafers are totally different from those in undoped SOI wafer (Figure 2.6). HD SOI wafers still show a small field-effect modulation of the drain current, which is also reflected by changes in the corresponding $g_m(V_G)$ curves (Figure 2.9b and d). Note that both drain current and transconductance have different variations between 0 ~ +40 V and 0 ~ −40 V, revealing two types of conduction mechanisms. The non-linear regions in Figure 2.9a and c indicate that an accumulation channel is activated (0 ~ +40 V for As-implanted and P-implanted samples and 0 ~ −40 V for B-implanted sample). For opposite gate biasing (0 ~ −40 V for As-implanted and P-implanted samples and 0 ~ +40 V for B-implanted sample), the films tend to be depleted, and a linear $I_D(V_G)$ dependence is observed.

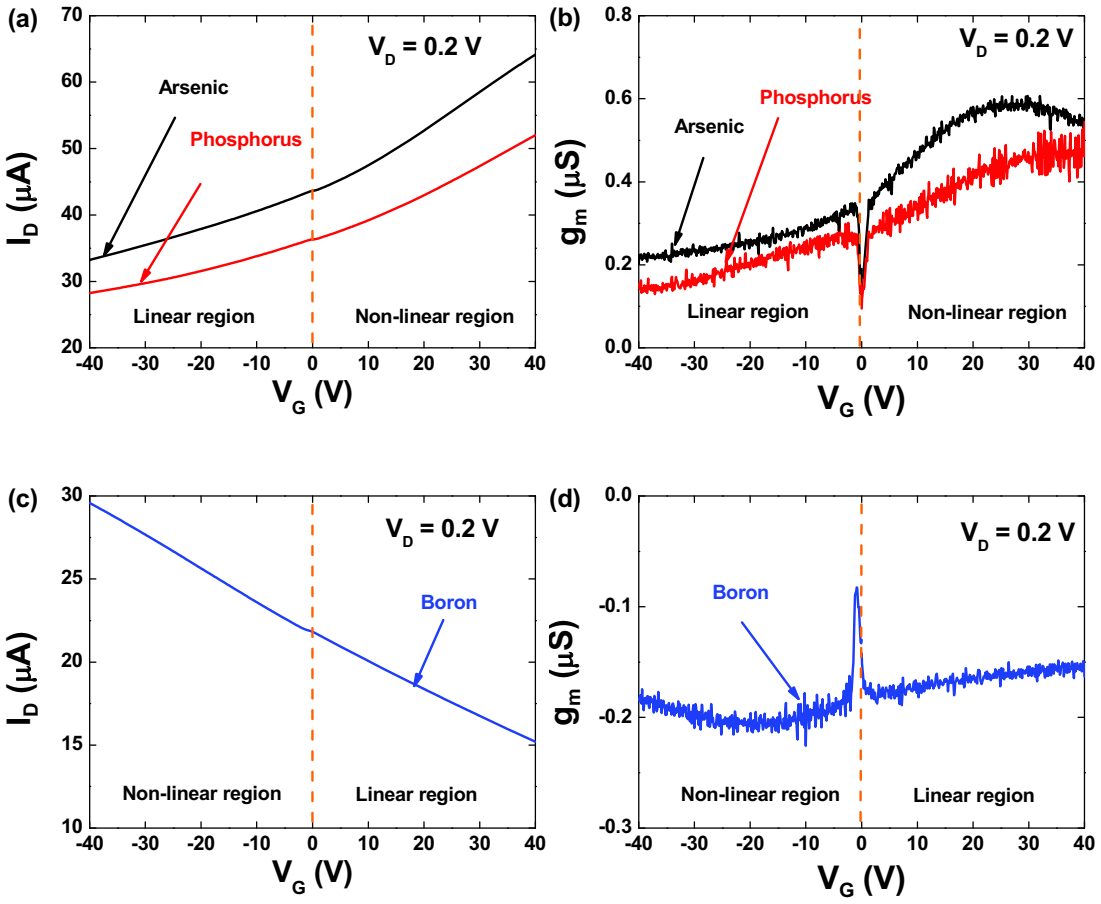

Figure 2.9: *Drain current and transconductance versus gate bias in 40 nm HD SOI wafers. (a) and (b) n-type implant; (c) and (d) p-type implant. Probe pressure = 60 g.*

The expansion of the depletion region, reflected by a linear decrease of volume current (linear region in Figure 2.9a and c), leads to a nearly constant transconductance (Figure 2.9b and d). Note that the heavily-doped films cannot be fully depleted: there is no zero-current region (as in Figure 2.6a for undoped SOI at $V_G \approx 0$ V). A neutral region with 'volume' conduction subsists for the entire V_G range. The current is exclusively due to majority carriers. No obvious inversion channel is obtained, which is possibly explained by a corresponding V_T value too high to be experimentally reached. The onset of the inversion channel would have been detected from the presence of a minimum current value, for $V_G \approx V_T$, beyond which the current would have increased due to the parallel conduction of minority and majority carriers.

Figure 2.10 gives the Ψ-MOSFET results for 10 nm HD SOI wafers. The field-effect modulation is even smaller compared with 40 nm HD SOI wafers, probably due to the higher doping level (10^{20} cm^{-3}). The drain current varies quasi-linearly with the gate voltage from −40 V to +40 V (Figure 2.10a and c), reflecting the linear expansion of the depletion region. The transconductances are rather constant, as shown in Figure 2.10b and d. As a result, only volume conduction appears in 10 nm samples and the formation of the depletion region is responsible for less than 10% current variation (the total variation in the whole region (−40 V ~ +40 V) divided by the maximum current, for example, (103 μA−94 μA)/103μA = 8.7% for arsenic-implanted samples).

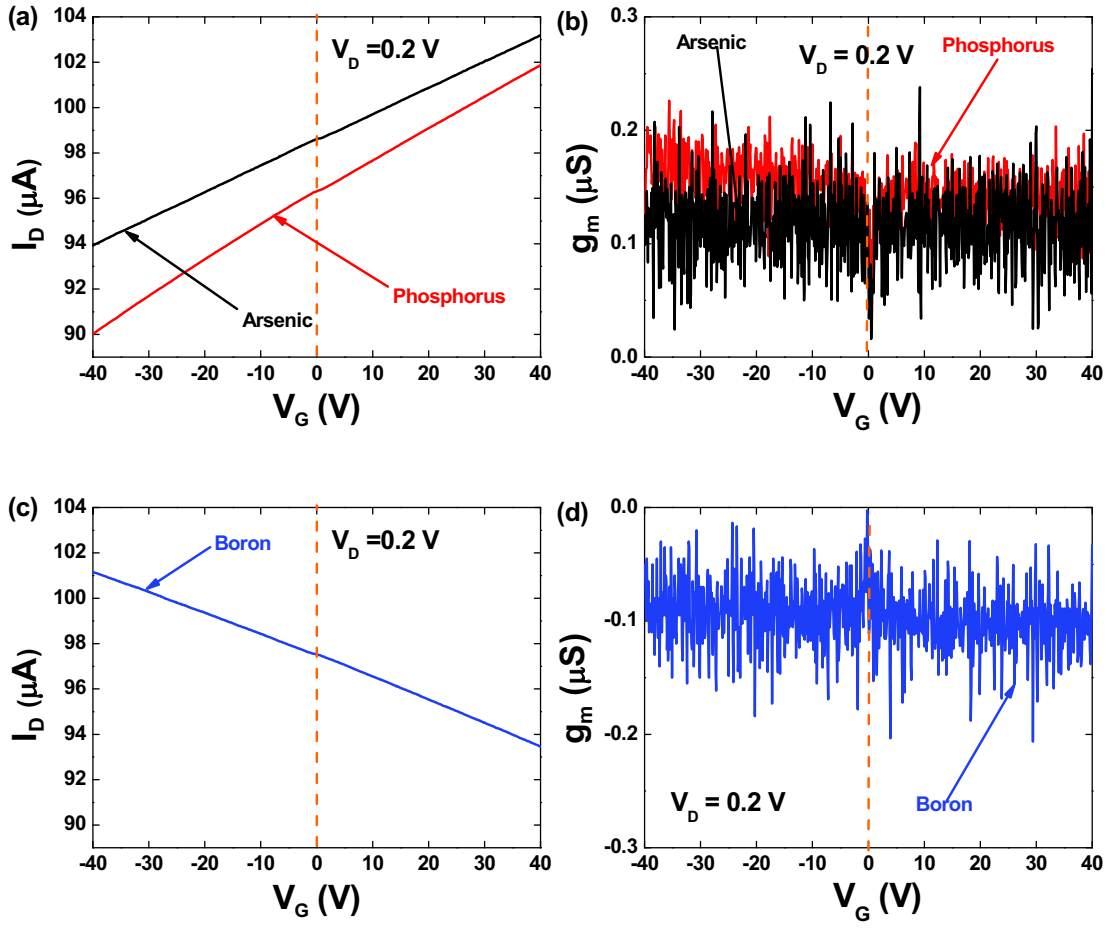

Figure 2.10: *Drain current and transconductance versus gate bias in 10 nm HD SOI wafers. (a) and (b) n-type implant; (c) and (d) p-type implant. Probe pressure = 30 g.*

2.3 Geometric factor for HD SOI wafers

Before modeling the Ψ-MOSFET in HD SOI wafers using the conventional Y-function (Eq. (2.3)), the geometric factor needs to be determined. According to [6], the geometric factor can be obtained from the comparison of point-contact Ψ-MOSFET and four-point probe measurements.

The configuration for four-point probe experiments is reminded in Figure 2.11. The probes are aligned and their pressure is of 60 g. The current is injected from probe 1 to probe 4 (I_{14}) and the voltage drop between the inner probes (V_{23}) is measured with a very high impedance voltmeter (1 GΩ). This eliminates the current flowing into probe 2 and probe 3. The sheet resistance is written as [19]:

$$R_{\square}(V_G) = 4.53 \times \frac{V_{23}}{I_{14}} \tag{2.4}$$

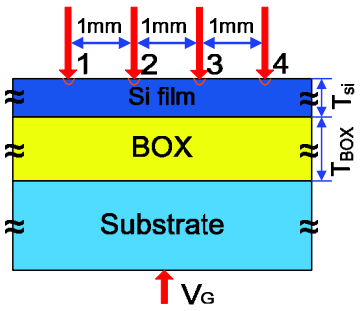

***Figure 2.11**: Schematic configuration for four-point probe measurements.*

Under Ψ-MOSFET configuration, the sheet resistance can be rewritten as [7], [20]:

$$R_{\square}(V_G) = f_G \frac{V_D}{I_D} \tag{2.5}$$

Combining Eqs. (2.4) and (2.5), the geometric factor can be calculated as:

$$f_G = 4.53 \times \frac{V_{23} I_D}{I_{14} V_D} = 4.53 \times \frac{V_{23} / I_{14}}{V_D / I_D} \tag{2.6}$$

Figure 2.12a compares I_D and I_{14} for 40 nm P-implanted SOI wafers with $V_G = 0$ V. f_G can easily determined from the ratio of the slopes of $I_{14}(V_{23})$ and $I_D(V_D)$ curves. Figure 2.12b shows the calculated geometric factor versus different gate voltage for 40 nm HD SOI wafers. The calculated geometric factor for HD SOI wafers is close to the classical value for undoped wafers. For simplicity, we will use 0.75 for all the characterization of HD SOI wafers, as in the undoped wafers.

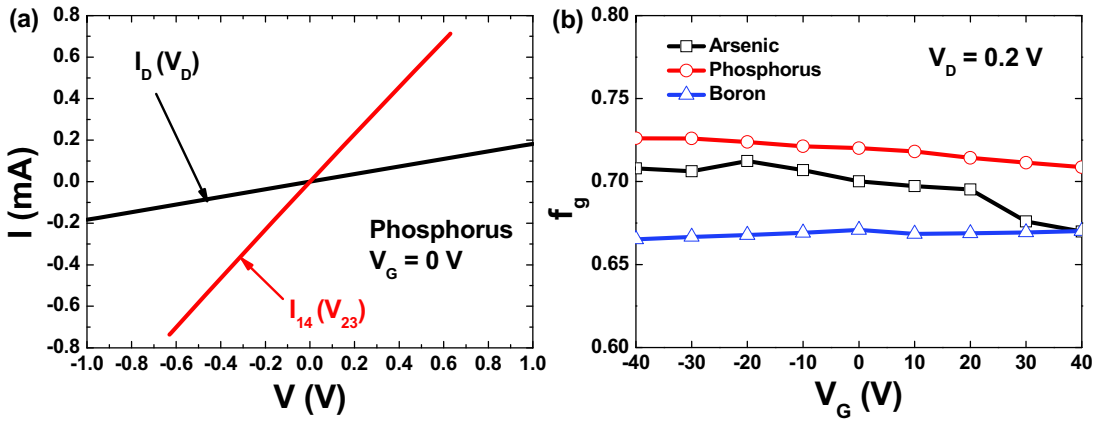

***Figure 2.12:** (a) Comparison of I_D and I_{14} for P-implanted SOI wafers with V_G = 0 V and (b) calculated geometric factor versus gate bias in 40 nm HD SOI wafers. Probe pressure = 60 g.*

2.4 Conventional Y-function for HD SOI wafers

The conventional Y-function in HD SOI wafers is given in Figure 2.13. No straight line $Y(V_G)$ is obtained, which makes the parameter extraction impossible. This problem was predictable, being attributed to the strong volume current masking the channel (unlike the case of undoped SOI wafers where $I_{vol} \approx 1$ pA at $V_G = 0$ V in Figure 2.6a). The classical MOSFET equations cannot be used here as in undoped SOI wafers. A revisited model for parameters extraction is needed and we describe ours in the next sub-section.

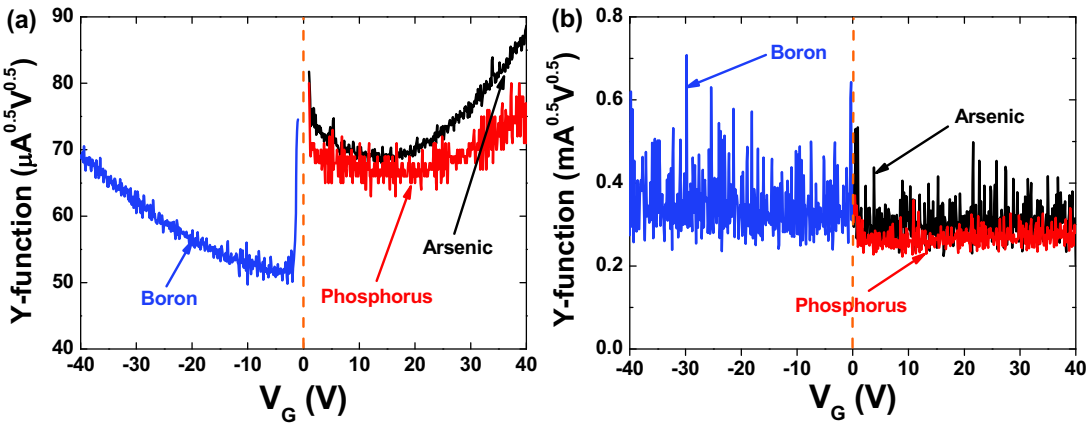

Figure 2.13: *Conventional Y-function using the total drain current for: (a) 40 nm and (b) 10 nm HD films.*

3. Revisited model for HD SOI wafers

Figure 2.9a shows the two conduction regimes involved in $I_D(V_G)$characteristics of heavily-doped substrates: (i) variable volume contribution assisted by the growth of the depletion region and (ii) interface accumulation [21]. In this section, analytical expressions are proposed for each region; they will be used later to extract the corresponding material parameters: flat-band voltage V_{FB}, interface mobility μ_s, volume mobility μ_{vol} for holes or electrons, and activated concentration for acceptors N_A or donors N_D.

3.1 Variable volume contribution

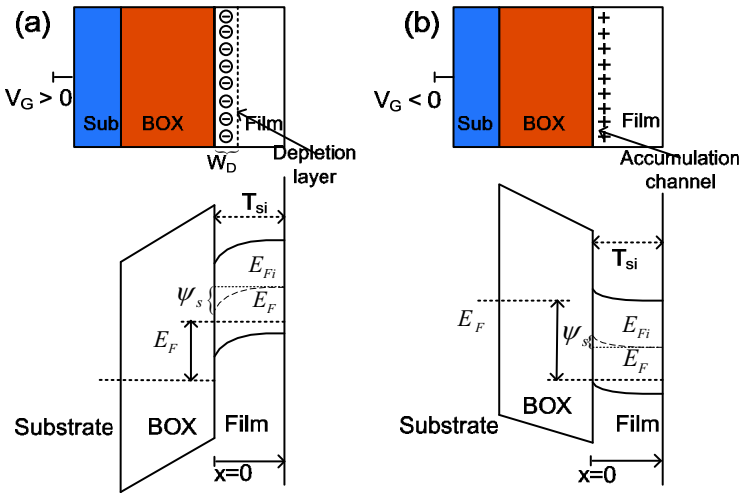

Figure 2.14: *Ψ-MOSFET cross section and energy-band structure in boron-implanted SOI wafers for (a) $V_G > 0$ and (b) $V_G < 0$. E_{Fi} denotes the intrinsic Fermi level, E_F denotes the Fermi level and ψ_s is the surface potential.*

When V_G is negative for n-type SOI or positive for p-type SOI, a depletion layer is formed at the Film/BOX interface, shown in Figure 2.14a. Depletion effect below the BOX and interface traps are neglected [22], so surface potential ψ_s at Film/BOX interface is mainly affected by gate bias. The coupling between front surface and the channel can be neglected in first-order approximation, because the film is not fully-depleted. We consider boron-implanted SOI wafer as example but a similar derivation is straightforward for donor-type doping (arsenic and phosphorus). If we focus on the depletion region only (from 0 to W_D), the Poisson equation for the silicon-film region can be written as:

$$\frac{d^2\varphi(x)}{dx^2} = \frac{q}{\varepsilon_{si}} N_A \tag{2.7}$$

Here, $\varphi(x)$ is the electrostatic potential in the Si film, q is the electron charge, ε_{si} is the permittivity of silicon and N_A is the concentration of acceptors in the Si film. Integrating Eq. (2.7) from 0 to W_D along x direction, the charge of depletion layer Q_D can be expressed as follows:

$$Q_D = -qN_A W_D = -\sqrt{2q\varepsilon_{si} N_A \psi_s} \tag{2.8}$$

The boundary condition at the Film/BOX interface can be established from Gauss law:

$$\varepsilon_{BOX}\frac{V_G - V_{FB} - \psi_s}{T_{BOX}} = C_{BOX}\left(V_G - V_{FB} - \psi_s\right) = -Q_D \tag{2.9}$$

in which ε_{BOX} and T_{BOX} are respectively the permittivity and thickness of BOX, C_{BOX} is the capacitance of BOX per unit area. Combining Eq. (2.8) and Eq. (2.9) yields the width of depletion layer W_D:

$$W_D = \frac{\varepsilon_{si}}{C_{BOX}}\left(-1+\sqrt{1+\frac{2C_{BOX}^2}{qN_A\varepsilon_{si}}\left(V_G - V_{FB}\right)}\right) \tag{2.10}$$

The second term under the radical sign is usually very small compared to 1 (0.03 for N_A = 10^{19} cm^{-3}, T_{BOX} = 145 nm and V_G–V_{FB} = 40 V). Therefore first-order approximation is valid and gives:

$$W_D = \frac{C_{BOX}}{qN_A}\left(V_G - V_{FB}\right) \tag{2.11}$$

Eq. (2.11) shows that the depletion layer is linearly increasing with V_G. Hence, the thickness of the conducting part of the film (T_{si}–W_D) decreases linearly with V_G. Assuming that the mobility in the film volume is constant, the drain current varies as a linear function of W_D:

$$I_D = I_{vol} = qf_G\mu_{p,vol}N_A(T_{si} - W_D)V_D \tag{2.12}$$

where $\mu_{p,vol}$ represents the mobility of holes in volume. Substituting Eq. (2.11) into Eq. (2.12), the volume current I_{vol} becomes:

$$I_{vol} = -f_G\mu_{p,vol}C_{BOX}(V_G - V_0)V_D \tag{2.13}$$

where V_0 is a characteristic voltage given by [21]:

$$V_0 = V_{FB} + \frac{qN_A}{C_{BOX}}T_{si} \tag{2.14}$$

V_0 represents a fictive voltage which would lead to full depletion of the film and is measured by extrapolating to zero the current in the linear region of $I_D(V_G)$ curves. Note that V_0 is very large (> 150 V) because the full depletion cannot be actually achieved due to the very high doping. V_0 yields the effective doping concentration N_A

using Eq. (2.14). The slope of Eq. (2.13) allows extracting the volume mobility μ_{vol}. Figure 2.15 shows the application of our model on the measured currents for 40 nm and 10 nm samples.

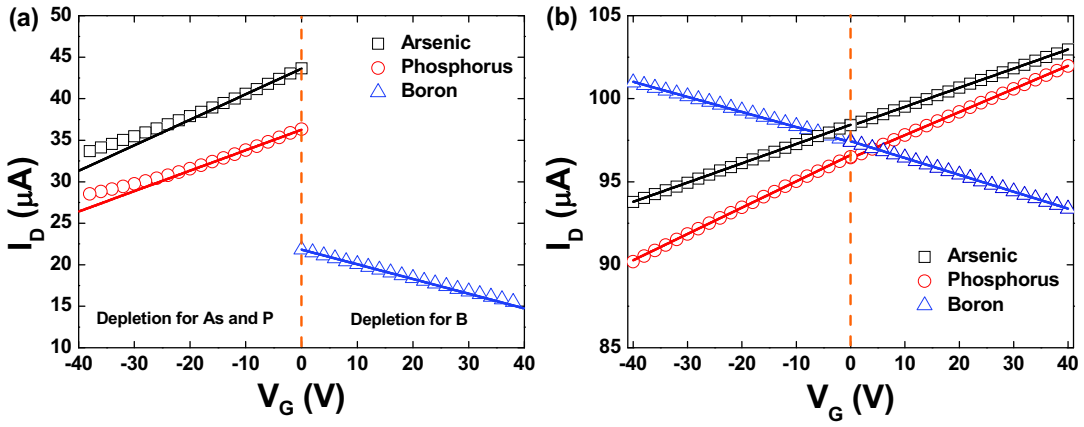

Figure 2.15: *Experimental and modeled drain currents in volume conduction regime of pseudo-MOSFET for (a) 40 nm and (b) 10 nm HD SOI wafers. Symbols: experimental data. Solid lines: model as in Eq. (2.13).*

For 40 nm HD wafers (Figure 2.15a), the model and experimental results match at relatively low voltage ($|V_G| < 20$ V). However, a small additional current is observed when $|V_G|$ increases from 20 V to 40 V for As- and P-implanted wafers. As we noted previously (Figure 2.9a), no strong inversion is observed in the $I_D(V_{FG})$ curves. Nevertheless, is the extra current induced by the formation of a weakly inverted channel? The threshold voltage is the critical voltage to distinguish strong and weak inversion conductance. In our HD samples, the threshold voltage is essentially governed by the maximum depletion charge:

$$V_T \approx \frac{qN_{A,D}W_{Dmax}}{C_{BOX}} \tag{2.15}$$

where W_{Dmax} is the maximum depletion width, given by [14]:

$$W_{Dmax} \approx \sqrt{\frac{2\varepsilon_{si}\psi_s}{qN_{A,D}}} \approx \sqrt{\frac{4\varepsilon_{si}kT\,ln(N_{A,D}/n_i)}{q^2N_{A,D}}} \tag{2.16}$$

If the implanted dopants are fully activated, the calculated threshold voltages are ~ 80 V for 10^{19} cm^{-3} doping and ~ 260 V for 10^{20} cm^{-3} doping. However, the actual doping concentration is lower due to the incomplete doping activation and can be obtained

from Eq. (2.14). For 40 nm samples, the extracted doping concentrations are 0.53 × 10^{19} cm^{-3} for arsenic and 0.52 × 10^{19} cm^{-3} for phosphorus. Therefore, the actual threshold voltage is lower. Weak inversion starts for lower surface potential ($\psi_s = \psi_F$) and may be expected for $V_G < 40$ V, so leading to extra current. No such effect can be observed in 10^{20} cm^{-3} doped films. Therefore, for 10 nm HD SOI wafers, the volume current calculated with Eq. (2.13) shows excellent agreement with the experimental data (Figure 2.15b): $I_D(V_G)$ curves are perfectly linear.

3.2 Interface accumulation

When V_G is positive enough for n-type SOI (negative for p-type SOI), an accumulation channel is formed at the Film/BOX interface (Figure 2.14b). As a result, the drain current contains the volume current and the accumulation current:

$$I_D = I_{vol} + I_{acc} \tag{2.17}$$

in which I_{vol} is the maximum volume current flowing through the entire, undepleted P-type Si film:

$$I_{vol} = qf_G\mu_{p,vol}N_AT_{si}V_D \tag{2.18}$$

The gate-dependent accumulation current I_{acc} is given by the classical expression of the MOSFET drain current in the ohmic regime [17]:

$$I_{acc} = -f_G C_{BOX}\frac{\mu_{p,s}}{1+\theta_{acc}(V_G - V_{FB})}(V_G - V_{FB})V_D \tag{2.19}$$

where $\mu_{p,s}$ is the interface mobility of the holes and θ_{acc} is the degradation factor of interface mobility.

In order to access the interface current only, we need to calculate the accumulation current from Eq. (2.17) ($I_{acc} = I_D - I_{vol}$). Theoretically, the volume current equals to the drain current measured at $V_G = V_{FB}$. We assume that the effect of traps at the Si/BOX interface on the flat-band voltage can be neglected. Therefore, the theoretical flat-band voltage mainly results from the work-function difference between the HD film and the P-type substrate:

$$V_{FB} = \frac{kT}{q}\ln\left(\frac{N_{sub}}{N_A}\right) \text{ for P-type film,}$$
$$V_{FB} = \frac{kT}{q}\ln\left(\frac{N_D N_{sub}}{n_i^2}\right) \text{ for N-type film} \quad (2.20)$$

where n_i is the intrinsic carrier density at room temperature (~ 1.5×10^{10} cm^{-3}) and N_{sub} is the doping concentration of substrate (~ 10^{15} cm^{-3}). Therefore, the calculated flat-band voltages for 40 nm HD films are: ~ 0.8 V for As- and P-implanted wafers and ~ −0.51 V for B-implanted wafers. Since all the theoretical flat-band voltages are close to 0, we uniformly use the drain current at V_G = 0 V to represent the volume current. The calculated accumulation current is given in Figure 2.16a.

We have seen in Figure 2.13 that the conventional Y-function cannot be applied to the total current. This is why we propose a new Y-function, Y_{acc}, is dedicated exclusively to the accumulation channel and is defined as:

$$Y_{acc} = \frac{I_D - I_{vol}}{\sqrt{g_m}} = \frac{I_{acc}}{\sqrt{g_m}} = \sqrt{f_G C_{BOX} V_D \mu_s}(V_G - V_{FB}) \quad (2.21)$$

Using the corrected Eq. (2.21), a linear variation of Y_{acc} versus V_G curve is obtained, as shown in Figure 2.16b for 40 nm heavily-doped SOI wafers. Note that this new Y-function is only applicable for the accumulation part of the curves. The mobility μ_s, extracted from the slope, is the majority carriers mobility at the Film/BOX interface and can be different from the volume mobility μ_{vol}. Note that at very high voltage, the new Y-function (open symbols in Figure 2.16b) is slightly higher than our model (solid lines in Figure 2.16b). This may possibly be explained by a gate-dependent screen effect [23]. The screen effect can enhance the interface mobility, which will be detailed in the next sub-section. In addition, we will discuss the other extracted parameters from Ψ-MOSFET experiments.

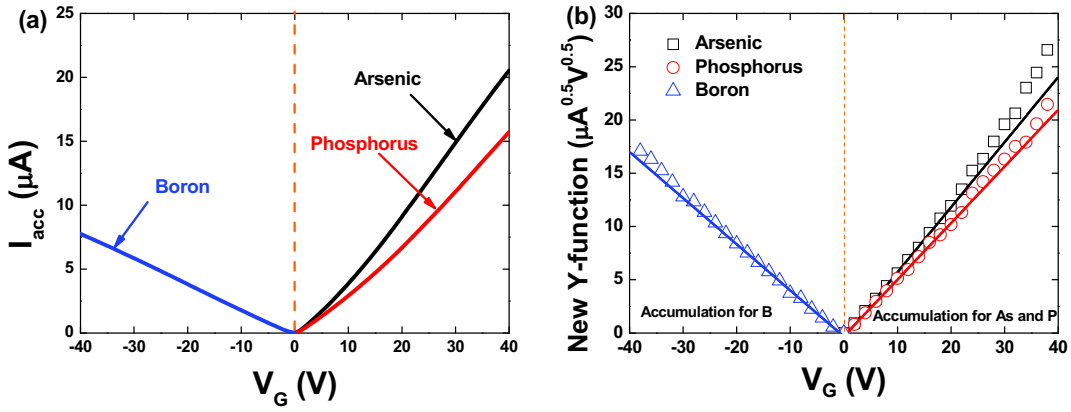

***Figure 2.16*:** *(a) Accumulation current and (b) revisited Y-function versus gate voltage for surface accumulation current. Symbols: experimental data for 40 nm heavily-doped SOI wafers. Solid lines: linear approximation using Eq. (2.21).*

3.3 Extracted results

Table 2-II summarizes the parameters (flat-band voltage, interface and volume mobility, doping concentration) extracted from Ψ-MOSFET measurements. The doping levels are close to the target values (10^{20} cm^{-3} for 10 nm samples and 10^{19} cm^{-3} for 40 nm samples). This implies that despite the very high implant doses, the impurities are essentially confined within the Si film (without significant diffusion into the BOX) and exhibit a reasonable electrical activation (~ 50%). The Secondary Ion Mass Spectroscopy (SIMS) profiles in Figure 2.17 confirm the rather uniform distribution of impurities (electrically active or not) in 40 nm thick films [24]. Only for P-implanted samples can a dopant segregation at the interface be observed.

***Table 2-II*:** *Extracted flat-band voltage, interface and volume mobility and activated doping concentration from Ψ-MOSFET data.*

Dopants	**40 nm (targeted doping ~10^{19} cm^{-3})**				**10 nm (targeted doping ~10^{20} cm^{-3})**	
	$N_{A,D}$ (10^{19} cm^{-3})	μ_{vol} (cm^2/Vs)	V_{FB} (V)	μ_s (cm^2/Vs)	$N_{A,D}$ (10^{20} cm^{-3})	μ_{vol} (cm^2/Vs)
undoped	-	-	−6.1 (V_{FB}) −6.9 (V_T)	94 (h) 457 (e)	-	-
Arsenic	0.53	86 (e)	0.68	104 (e)	1.3	32 (e)
Phosphorus	0.52	73 (e)	0.57	79 (e)	0.9	44 (e)
Boron	0.47	50 (h)	-0.77	53 (h)	1.4	28 (h)

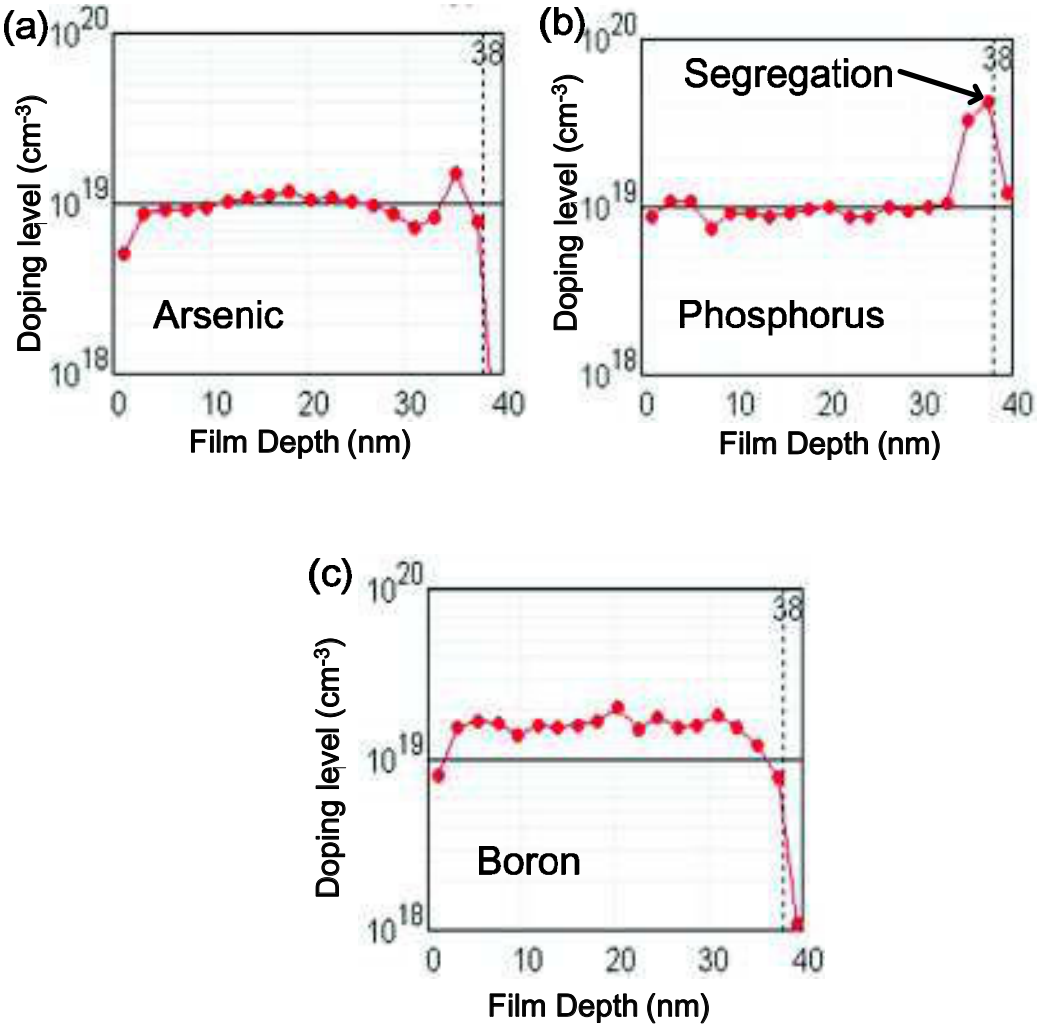

Figure 2.17**:** *SIMS doping profiles: (a) Arsenic, (b) Phosphorus and (c) Boron. The surfaces of the Si films are at zero depth (Courtesy of K. Akarvardar and C. Hobbs) [24].*

The mobility values in Table 2-II are much lower than those measured in the undoped wafer (Figure 2.7), which documents the strong reduction of the mobility (5x for electrons and 2x for holes) with doping level (10^{19} cm^{-3}). In the higher doped 10 nm thick films, the mobility is further reduced by a factor of two. The mobility in the accumulation channel is systematically larger than in the volume. This can be interpreted by the accumulation channel screening the effect of Coulomb scattering on interface mobility [23], [25], [26]. In heavily-doped devices (10^{19} cm^{-3} or above), mobility is dominated by Coulomb scattering rather than by phonon or surface roughness scattering [27]. With the majority carrier (electrons concentration at the Film/BOX interface increasing in weak accumulation mode, a neutralizing screen around the positively-charged, ionized donor or acceptor atoms is created. This screen can reduce the cross-section of Coulomb scattering, enabling higher interface mobility

than bulk mobility. This screen effect was also demonstrated in heavily-doped junctionless transistors [28].

Although the 40 nm thick samples were implanted with the same dose, P-implanted wafers show lower mobility than in As-implanted wafers. The difference in interface mobility (−25%) is attributed to the segregation of phosphorus atoms at the back interface during annealing (Figure 2.17b). This segregation leads to higher impurity concentration at the Film/BOX interface for P-implanted wafers, enabling stronger Coulomb scattering.

The extracted flat-band voltages in Table 2-II are small. As calculated previously, the theoretical values of flat-band voltages are ~ 0.8 V for As- and P-implanted wafers and ~ −0.51 V for B-implanted wafers. Some deviations may result from a concentration of interface and oxide defects, which were neglected in the calculations. Nevertheless, the extracted flat-band voltages are still close to the theoretical values, demonstrating that the implantation process did not degrade the interface quality [29], [30].

In addition, using the drain current at the extracted flat-band voltage as volume current and the doping level extracted from V_0, we can easily calculate the volume mobility from Eq. (2.18). We obtain 86 cm^2/Vs for As-doped wafers, 73 cm^2/Vs for P-doped wafers and 49 cm^2/Vs for B-doped wafers (Table 2-II).

4. Van der Pauw and Hall effect

In order to confirm our novel MOSFET extraction method for HD SOI wafers, we also performed Van der Pauw and Hall effect measurements, which provide independently the mobility and doping level.

4.1 Experiments setup

Figure 2.18 shows the experimental platform and configuration for Van de Pauw and Hall effect measurements with four pressure probes in the corners of the die. In our home-made system, the die is placed on a metal support (for back-gate biasing) which can be gently moved into the center of the magnet gap. The direction of the magnetic field B can be reversed. The measurement is computer controlled and automated.

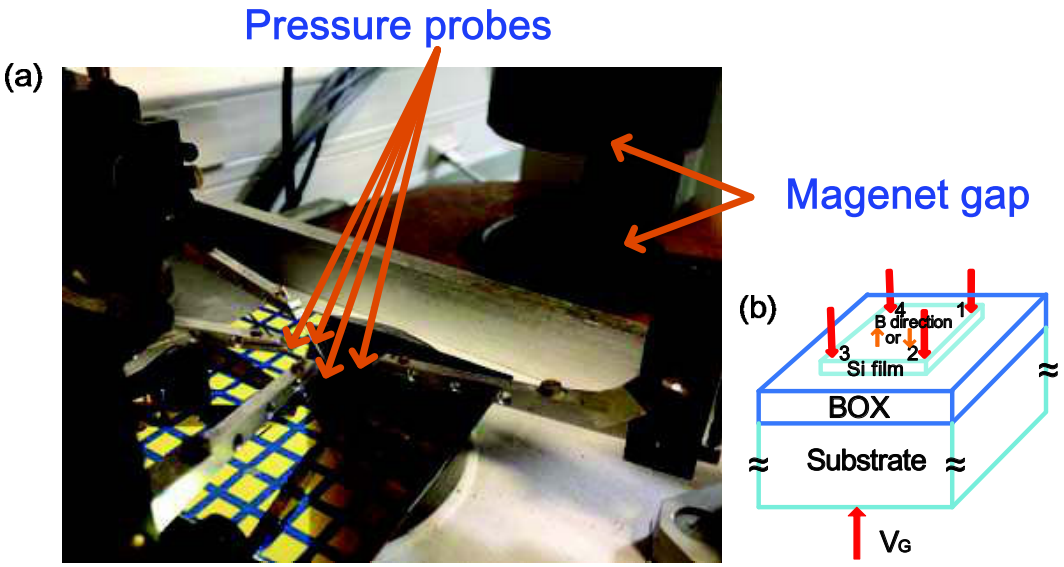

Figure 2.18: *(a) Experimental platform and (b) schematic configuration for Van de Pauw and Hall effect.*

Before Hall effect measurements, contact resistance experiments are performed in order to verify whether all the contacts are ohmic. Then, Van der Pauw experiments at $B = 0$ yield the average resistivity ρ_{VDP} [17]:

$$\rho_{VDP} = \frac{\pi T_{si}}{\ln 2} \times \frac{R_{12,34} + R_{23,41}}{2} \times f \tag{2.22}$$

where $R_{12,34}$ and $R_{23,41}$ are pseudoresistances, defined as $R_{12,34} = \frac{V_{34}}{I_{12}}$ and $R_{23,41} = \frac{V_{41}}{I_{23}}$, respectively. V_{34} corresponds to the voltage measured between probe 3 and probe 4 when the current I_{12} is injected through probe 1 and probe 2. Similar definitions apply to V_{41} and I_{23}. T_{si} is the film thickness and f is a configuration coefficient given by [17]:

$$2\exp\left(-\frac{\ln 2}{f}\right) \times \cosh\left(\frac{R_{12,34}/R_{23,41} - 1}{R_{12,34}/R_{23,41} + 1} \times \frac{\ln 2}{f}\right) = 1 \tag{2.23}$$

For additional accuracy, the Van der Pauw measurements are repeated by injecting the current from probe 3 to probe 4 and from probe 4 to probe 1. The final resistivity is the average value.

For the Hall effect measurements, 0.5 T magnetic field is applied vertical to the dies. The current is injected from probe 1 to probe 3 (I_{13}) and the corresponding voltage between the two other probes (probe 2 and probe 4) is measured. The measurement is repeated by (i) injecting from probe 3 (I_{31}) and (ii) reversing the magnetic field. The Hall voltage V_H can be calculated as:

$$V_H = \frac{V_{24}(I_{13},+B) - V_{24}(I_{31},+B) + V_{24}(I_{31},-B) - V_{24}(I_{13},-B)}{4} \tag{2.24}$$

Here, $V_{24}(I_{13},+B)$ and $V_{24}(I_{31},+B)$ are the voltages between probe 2 and probe 4 when the current is injected from probe 1 and from probe 3, respectively. $V_{24}(I_{13},-B)$ and $V_{24}(I_{31},-B)$ are the measured voltages with the reversed magnetic field direction. For the sake of accuracy, the current is also injected into probe 2 or probe 4 and the corresponding voltages between probe 1 and probe 3 are detected. These measured values are cross-checked for consistency. The average values represent the final Hall voltage V_H and Hall current I_H from which the Hall coefficient R_H and Hall mobility μ_H can be extracted using standard expressions [17]:

$$R_H = -\frac{V_H \times T_{si}}{I_H \times B} \tag{2.25}$$

$$\mu_H = \frac{|R_H|}{\rho_{VDP}} \tag{2.26}$$

The doping concentration can be obtained from:

$$N_{A,D} = \frac{1}{q\rho_{VDP}\mu_H} \tag{2.27}$$

In next sub-section, we will discuss the extracted results from Hall effect.

4.2 Experimental results

Table 2-III gives the measured data from Hall effect experiments with $V_G = 0$ (maximum volume conduction). The overall agreement with Ψ-MOSFET results (Table 2-II) is excellent. This indicates that the Ψ-MOSFET delivers reliable results. It is the only transport method that is able to provide independently the carrier

concentration (from V_0, Eq. (2.14)) and mobility (from Eqs. (2.13), (2.18) or (2.21)) without the need of a magnetic field. It follows that the Ψ-MOSFET can be substituted to the more tedious, time-consuming Hall effect measurements.

Table 2-III: *Extracted volume mobility and activated doping concentration from Hall effect (V_G = 0 V) and Ψ-MOSFET measurements.*

Dopants	40 nm				10 nm			
	$N_{A,D}$ (10^{19} cm^{-3})		μ_H *or* μ_{vol} (cm^2/Vs)		$N_{A,D}$ (10^{20} cm^{-3})		μ_H *or* μ_{vol} (cm^2/Vs)	
	Hall	**Ψ-MOSFET**	***Hall***	**Ψ-MOSFET**	***Hall***	**Ψ-MOSFET**	***Hall***	**Ψ-MOSFET**
Arsenic	0.58	0.53	108 (e)	86 (e)	1.4	1.3	43 (e)	32 (e)
Phosphorus	0.46	0.52	107 (e)	73 (e)	0.97	0.9	62 (e)	44 (e)
Boron	0.62	0.47	55 (h)	50 (h)	2.9	1.4	22 (h)	28 (h)

The mobility comparison between Ψ-MOSFET and Hall effect offers additional information on the scattering mechanisms. The Hall mobility (Table 2-III) is consistently larger than the volume drift mobility calculated in depletion (Eq. (2.13), Table 2-II). The difference between Hall and volume mobilities results from the combination of Coulomb and phonon scattering. It is known that the Hall scattering factor $r_H = \mu_H/\mu_{vol}$ equals to 1.93 for Coulomb scattering and 1.18 for acoustic phonons scattering [17]. In our 10^{19} cm^{-3} samples, $r_H \approx$ 1.1-1.3 shows the prevailing role of phonon scattering. In 10^{20} cm^{-3} samples, r_H increases to 1.5 as a consequence of stronger Coulomb scattering. An exception is observed only for B-doped 10 nm films: r_H = 0.79. This can be probably attributed to overestimated geometric factor for B-doped films. Figure 2.12b shows that the actual geometric factor is ~ 0.67 for B-doped 40 nm wafers, lower than 0.75 used for extraction in Ψ-MOSFET. The geometric factor for 10 nm wafers cannot be obtained due to the breakdown of BOX in four-point probe measurements.

The Hall effect measurement can also be performed with different gate biasing, as shown in Figure 2.19. In variable volume conduction mode (−40 V to 0 V for arsenic- and phosphorus-implanted wafers; 0 V to +40 V for boron-implanted wafer), the Hall mobility keeps constant. In interface accumulation mode, the Hall mobility increases with the $|V_G|$ rising, especially for As- and P-doped SOI wafers; for B-doped films,

more negative gate bias is needed to exhibit higher mobility. The mobility enhancement in accumulation can be attributed to the screen effect, which corresponds to the results extracted from Ψ-MOSFET (Table 2-II).

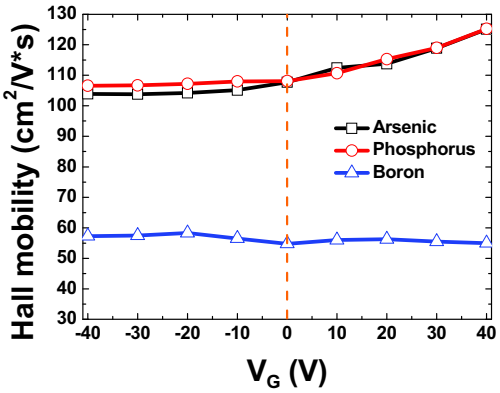

Figure 2.19**:** *Hall mobility versus back-gate bias, from Van der Pauw measurements on 40 nm heavily-doped SOI wafers.*

4.3 Resistivity comparison

According to [17], the average resistivity extracted from Ψ-MOSFET can be calculated as:

$$\rho = \frac{1}{qN_{A,D}\mu_{vol}} \tag{2.28}$$

For four-point probes experiments, the average resistivity can be determined from the sheet resistance:

$$\rho = R_{\square} T_{si} \tag{2.29}$$

Table 2-IV compares the resistivities extracted from Ψ-MOSFET, Van der Pauw and four-point probes measurements. The results show convincing agreement, although the four-point probe is unable to separate the carrier mobility and concentration.

Table 2-IV**:** *Resistivities in HD SOI wafers measured with different methods.*

Dopants	10 nm			40 nm		
	Ψ-MOSFET	VDP	4-point probe	Ψ-MOSFET	VDP	4-point probe
	ρ (cm · Ω)	ρ (cm · Ω)	ρ (cm · Ω)	ρ (cm · Ω)	ρ (cm · Ω)	ρ (cm · Ω)
Arsenic	0.0015	0.0010	0.0014	0.014	0.010	0.013
Phosphorus	0.0016	0.0010	0.0013	0.016	0.012	0.016
Boron	0.0016	0.0010	0.0014	0.027	0.018	0.025

5. Conclusions and perspectives

In this chapter, we showed for the first time that the Ψ-MOSFET technique can be adapted for HD SOI wafers. The field-effect induced by back-gate biasing is small, due to very high implanting dose, but it is still exploitable for detailed characterization. The volume conductance is modulated by the variation of the depletion region and dominates the total current. In samples with 10^{19} cm^{-3} doping, an accumulation channel is formed and gives insight on the carrier mobility at the Film/BOX interface. By contrast, only the volume mobility can be detected in 10^{20} cm^{-3} doped samples.

Unlike the case of undoped wafers, the volume current prevails in HD SOI. We showed that parameters extraction is possible using an updated model which takes the volume currents into account. As the Ψ-MOSFET yields the carrier mobility (in volume and at the interface) and the doping concentration independently, it can successfully replace more complex Hall effect measurements. This conclusion has been validated by comparing Ψ-MOSFET, Hall and four-point probe experiments.

Our results have key technological implications. Firstly, we showed that ultra-thin Si films can be efficiently doped up to at least 10^{20} cm^{-3}, with good dopant activation and confinement in the film. This kind of high doping can be used for the source/drain engineering in ultra-thin fully depleted SOI MOSFETs or FinFETs, enabling a lower access resistance. Secondly, it was found that 10 nm films with 10^{20} cm^{-3} doping cannot be fully depleted and a large volume current subsists. Since film thinning below 3-5 nm is still challenging, the doping of the body needs to be reduced in the planar juncitonless transistors (10^{18}-10^{19} cm^{-3}) in order to be able to switch off the channel. However, this lower-doping level cannot be used for source and drain due to large access resistance. Therefore, higher doping concentration (10^{20} cm^{-3}) is used for source and drain in planar junctionless transistors [31]. This will lead to the formation

of junction between body and source/drain. Such a 'junction-engineered junctionless transistor' actually belongs to the family of highly doped accumulation-mode MOSFETs. Another choice for junctionless transistors is the design of multiple-gate, such as junctionless FinFET [32], where the depletion region is expanded.

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Chapter 3: Characterization of metal bonded silicon wafers

Three-dimensional (3D) integration is the final solution to overcome the challenges of "More Moore" applications [1]. It is an advanced technology, integrating two or more layers of active electronic components both vertically and horizontally into a single chip. These layers include dissimilar materials, process technologies and functionalities [2]. Many methods have been proposed to achieve 3D integration [3], [4]: monolithic growth or wafer-to-wafer, die-to-wafer and die-to-die. Direct wafer-to-wafer bonding has shown a compelling advantage in terms of bonding quality and mechanical attachment, alignment capability, reliability and cost [5], [6]. Many applications based on wafer bonding have been demonstrated: Micro Electro Mechanical Systems [7], hetero integration [8]–[10], interconnection and packaging by Through Silicon Via (TSV) [11]–[15]. For example, IBM recently reported 2.1 GHz 3D stacked embedded DRAM in 45 nm SOI technology node based on low-temperature oxide bonding and copper TSVs [16].

Though owing so many attractive advantages, wafer bonding technology still faces some challenges [4], such as heat dissipation, design complexity and bottleneck of conventional testing technology. Indeed, one of the key issues when fabricating bonded wafers is to insure low impact of the bonding process on the devices. The metal-to-metal bonding is important for achieving high quality interconnection and novel devices. The need for an electrical technique which gives quantitative information about the bonding quality is obvious.

In this chapter, the electrical characteristics for metal-bonded wafers are investigated. Based on TCAD simulations and experimental results, the resistance assessing the bonding interface is extracted. We investigate the resistance variation as a function of the technological options.

1. State-of-the-art for characterization of metal bonded wafers

For high-quality bonding, smooth metal surfaces (atom-level clean) are demanded. The plastic deformation of the metal brings two wafers together in atom-close contact. Despite maintaining clean surfaces of metal, intrinsic or extrinsic voids can still be generated when bonding and annealing a wafer pair [17], [18]. Therefore, it is essential to assess the bonding quality before completing device fabrication [19]. Many methods have been reported to characterize the voids and their effect. The methods mainly include cross-sectional analysis (such as Scanning Electron

Microscopy (SEM) [20], Transmission Electron Microscopy (TEM) [20]–[22], Auger electron spectroscopy [23], *etc.*) and bond-strength measurement. Note that all these methods are destructive.

On the other hand, most nondestructive methods involve bonding imaging: infrared transmission, Scanning Acoustic Microscopy (SAM) [24] and X-ray topography. These nondestructive methods are expensive, complicated and time-consuming. More importantly, they do not reveal the electrical performance of the bonding interface.

Besides mechanical strength and interfacial defects, the primary concern for bonding interface is the electrical contact resistance. F. Shi *et al.* proposed an $I(V)$ method to assess the electrical quality of bonded p-n junctions in bonded GaAs wafers [25]. F. Gity *et al.* analyzed the current transport across a p-Ge/n-Si diode structure obtained by direct wafer bonding [26]. However, these two electrical characterizations require a p-n junction or heterojunction at the bonding interface.

For metal-bonded wafers, no junction exists at the bonding interface. Therefore, a specific Kelvin cross was proposed to directly measure the contact resistance for bonded interface, as shown in Figure 3.1a [21], [27]. The current is injected with two contact tips and forced to flow through the bonding interface. Two other tips measure the drop of voltage at the bonding interface. At first approximation, the contact resistance R_C can be calculated as:

$$R_C = \frac{V_{MT} - V_{MB}}{I} \tag{3.1}$$

where V_{MT} and V_{MB} are respectively the measured voltages of top and bottom layers and I is the corresponding current. This method needs to etch the top layer for fabrication of the Kelvin cross. In this chapter, we propose a simpler and faster method that does not need any technological process: the direct current-voltage measurement across the bonded wafers.

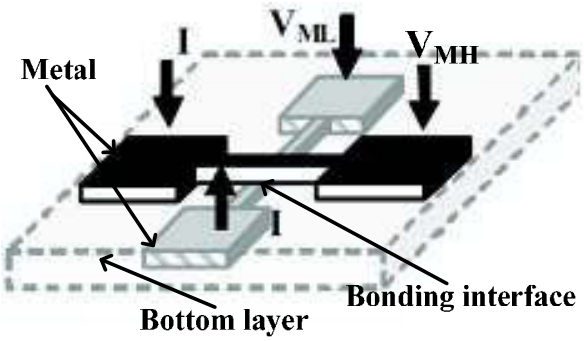

Figure 3.1: *Schematic of Kelvin cross for measuring the contact resistance [21].*

2. Experiments set up

2.1 Sample preparation

Two types of metal-to-metal bonded wafers were fabricated at CEA-Leti, as described in Figure 3.2. A 60 nm titanium nitride (TiN) layer was firstly deposited on two 12-inch bare silicon wafers (boron-doped, 5×10^{14} cm^{-3}, 725 µm thickness) as buffer to prevent the bonding metal diffusing into the silicon film. Then, a thin titanium layer was deposited on the TiN layer. The titanium surfaces of both wafers were cleaned (atom-level) and then mechanically bonded together at room temperature (RT). All the samples used in the measurements are detailed in Table 3-I. The two bonded samples (Bond10 and Bond5) are fabricated with the thickness of titanium layer of 10 nm and 5 nm, respectively. Two splits were measured: one with wafers annealed at 400°C for two hours and the other without annealing (here called RT wafers). The bare silicon wafer without bonding (Bare) was used as a reference.

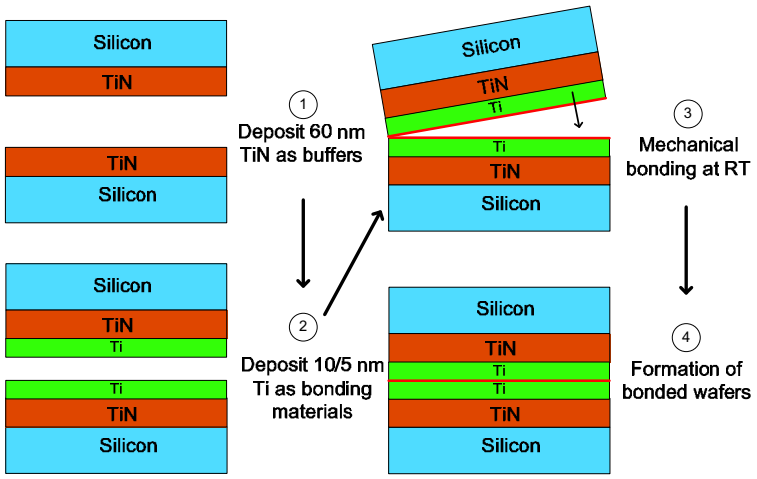

Figure 3.2: *Schematic of direct metal-bonded procedure.*

Table 3-I: *Different interlayers for the tested wafers*

Samples	Interlayers structure
Bond10	TiN (60 nm) / Ti (10 nm) — Ti (10 nm) / TiN (60 nm)
Bond5	TiN (60 nm) / Ti (5 nm) — Ti (5 nm) / TiN (60 nm)
Bare	Bare Si wafer

2.2 Experimental configuration

The standard Jandel Universal Probe Station was employed to perform the measurement, but only one pressure-controlled probe was placed on the top side of bonded wafers disposed on the copper chuck, as shown in Figure 3.3. All the experiments were conducted on 1 cm × 1 cm pieces to avoid edge leakage effects. The voltage between the probe and chuck is swept from −40 V to +40 V and the probe current was measured with a medium integration time. The hold time and delay time were respectively 5 s and 0.02 s. Two types of electrical configurations can be used: probe grounded or chuck grounded. All the measurements were performed with Agilent 4156B Semiconductor Analyzer at room temperature.

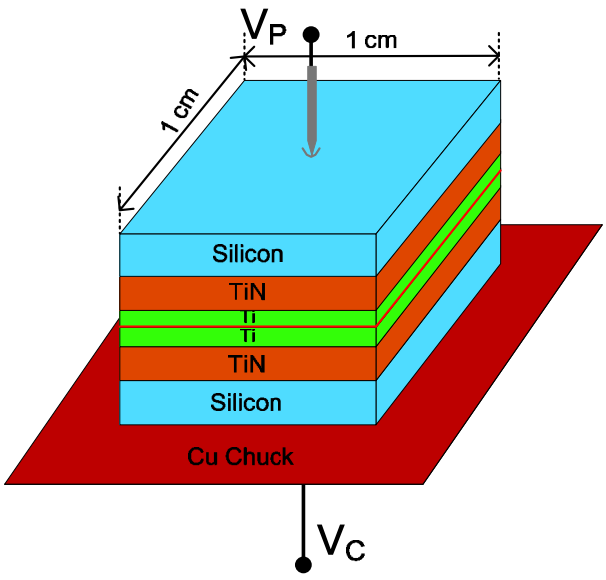

Figure 3.3: *Schematic configuration of I(V) measurements. V_P and V_C denote the voltage of probe and chuck, respectively.*

2.3 Experimental results

2.3.1 Bare wafers

Before testing metal bonded wafers, we firstly measured the bare Si wafer using the same configuration as shown in Figure 3.3. Figure 3.4a shows the current measured when the voltage is applied on the probe (V_P) and the chuck is grounded. The absolute value of probe current increases exponentially with negative V_P, and saturates at a low value for positive voltage range. With the probe pressure increase, the probe current for negative bias is enhanced. When the voltage is input from the chuck (V_C) and the probe is grounded, the exponential increase of probe current happens for positive bias (Figure 3.4b). With the chuck negatively biased, the probe current saturates only for 30 g; larger pressures enable higher current flow. The characteristics measured are not linear and they remind junction-type measurements. This is not surprising since the bare wafer in the configuration of Figure 3.3 involves metal-semiconductor contacts (Schottky junctions).

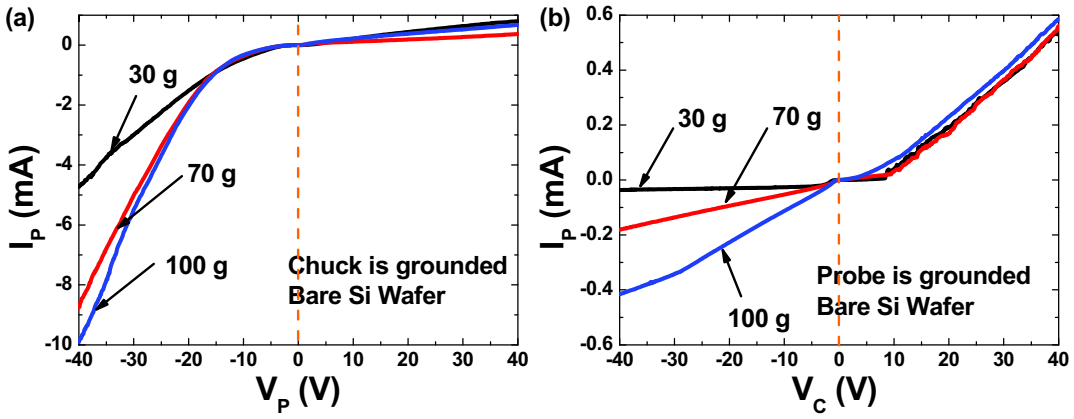

Figure 3.4: *Experimental I(V) curves for bare wafer. (a) The voltage is applied on the probe and the chuck is grounded; (b) the voltage is applied on the chuck and the probe is grounded.*

For the bare wafer, two Schottky contacts exist: probe/silicon (D_1) and silicon/chuck (D_2), as shown in Figure 3.5a. Without applied voltage, a Schottky barrier exists due to the difference of work-functions between silicon and metal. Assume that the metal/semiconductor is perfect and there are no traps at the Schottky contact. The barrier height ϕ_B for such an ideal Schottky contact is given by [28]:

$$\phi_B = E_g + \chi - \Phi_M \tag{3.2}$$

Here, χ and E_g are respectively the electron affinity (4.05 eV) and band gap (1.12 eV) of silicon; Φ_M is the work-function of the metal. According to [29], the work-functions for tungsten (probe) and copper (chuck) are respectively 4.55 eV and 4.65 eV. Therefore, the calculated barrier heights for D_1 and D_2 are: $\phi_{B\_D_1}$ = 0.62 eV and $\phi_{B\_D_2}$ = 0.52 eV. In addition, D_1 is a point-contact diode while D_2 has a large contact area. Therefore, D_1 (probe/silicon junction) has a higher energy barrier and a much smaller area than D_2 (silicon/chuck junction). We expected the current to be limited by D_1. Note that those remarks are consistent with the $I(V)$ curves in Figure 3.4a, in which the D_1 junction is biased (probe biased and chuck grounded). Indeed, negative V_P under this configuration corresponds to forward-biasing of D_1. For positive V_P, D_1 is reverse-biased and therefore I_P is limited. For all the next experiments, we will use this electrical configuration (chuck grounded). We will prefer using the highest probe pressure (100 g) in order to reduce the access resistance.

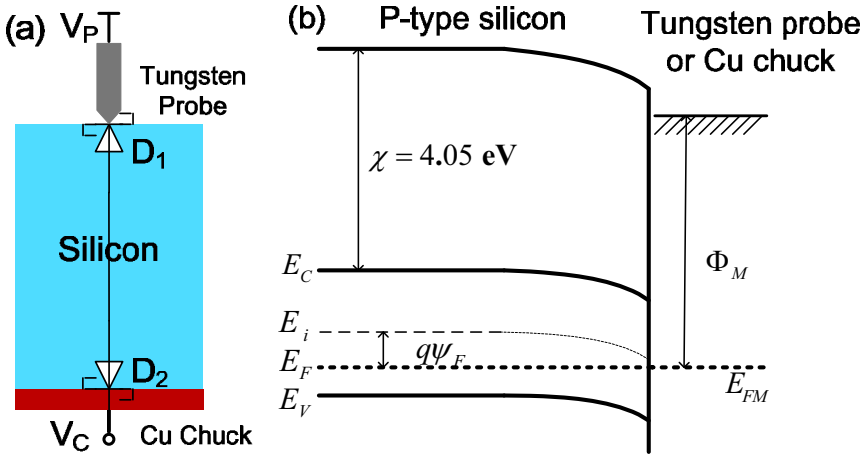

Figure 3.5: *(a) Cross-section of bare Si wafer with two Schottky contacts (D_1 and D_2) and (b) energy band for the Schottky contact without applied voltage.*

2.3.2 Bonded wafers

As seen in the previous section, we polarize the probe and ground the chuck. The probe pressure is set at 100 g. Figure 3.6 shows the measured $I_P(V_P)$ for bonded wafers: (a) Bond10, with 10 nm Ti as bonding layer and (b) Bond5, with 5 nm Ti as bonding layer. The open symbols show the curves obtained for samples without annealing ("RT") and the solid lines were obtained for samples with annealing at 400°C for 2 hours. First remark is that the current level is smaller than the one

obtained for Bare (Figure 3.4a). Nevertheless, the shape of the curves for non-annealed (RT) bonded wafers is similar to the one for Bare, suggesting a Schottky contact. The question is which Schottky contact dominates the transport here. Indeed, bonded wafers add four more interfaces besides probe/silicon and silicon/chuck, as shown in Figure 3.7. Since TiN is a titanium alloys with low electrical resistivity (~ 70 μΩ·cm) [26-27], we regard the two interfaces of Ti/TiN as ohmic contacts. Thus, only two extra Schottky junctions need be taken into account for bonded wafers: silicon/TiN (D_3) and TiN/silicon (D_4). The measured Schottky barrier of a TiN/p-type Si(100) junction is 0.53 V at room temperature [32], which is smaller than the one for Probe/Silicon Schottky contact (D_1). This means that the point-contact D_1 in bonded wafers will still dominate the $I_P(V_P)$ behavior, as in bare Si wafer.

The second remark is that after annealing at 400°C for 2 hours, both currents (especially the saturation current for positive voltage range) increase, clearly showing that the annealing decreases the resistance of the contacts.

The aim for these measurements is to find a parameter (possibly a resistance value) to quantify the impact of the annealing on the bonded wafers. In the next section, we will use TCAD simulations to validate our experimental results and propose an appropriate method of contact evaluation.

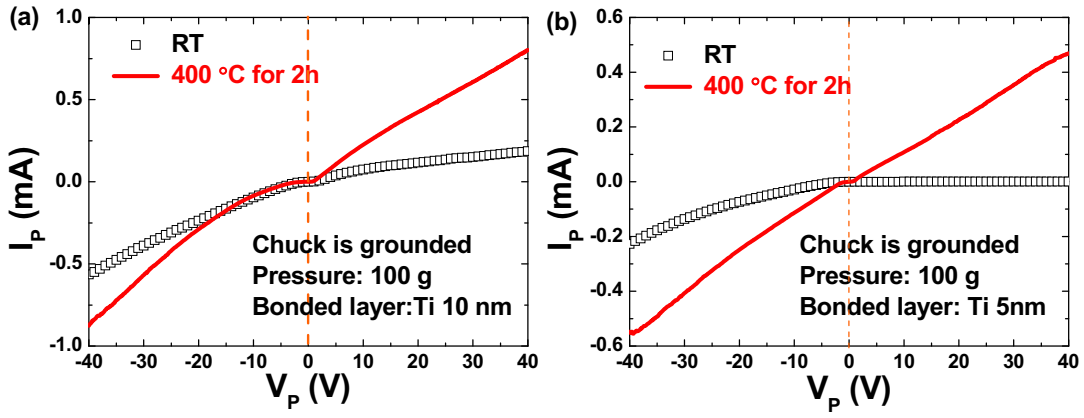

Figure 3.6: *Measured $I_P(V_P)$ curves for bonded wafers: (a) Bond10 and (b) Bond5.*

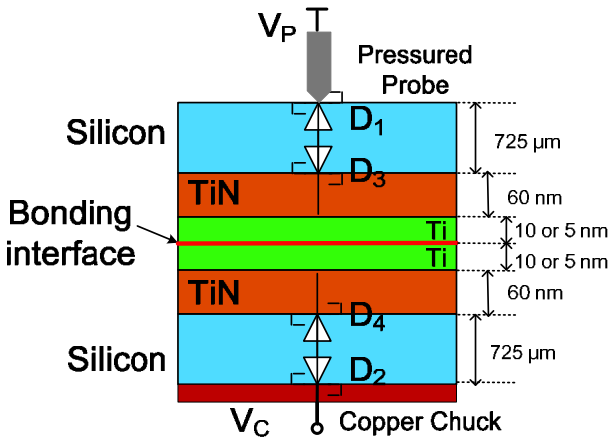

Figure 3.7: *Cross-section of bonded Si wafer with four Schottky contacts (D_1, D_2, D_3 and D_4).*

3. TCAD simulation

3.1 Employed models

Synopsys Sentaurus TCAD is employed to reproduce the $I(V)$ curves for bare and bonded wafers [33]. Fermi-Dirac statistics is used to calculate the densities of carriers. The Philips Unified Mobility Model is used, which mainly considers the phonon scattering, Coulomb scattering and electron-hole scattering. Model for velocity saturation due to high electric field is also included.

3.2 Simulation results

3.2.1 Bare wafers: Schottky contact

- **Simulation setup**

The measured sample for bare silicon is a cuboid with the area (S) 1 cm^2 and thickness (T_{si}) 725 µm. Since the current flows between probe and chuck, the theoretical resistance R_{Si} can be calculated as:

$$R_{Si} = \rho \frac{T_{si}}{S} \tag{3.3}$$

where ρ is the resistivity for silicon. The resistivity for the p-type wafer ($N_A = 5 \times 10^{14}$ cm^{-3}) is ~ 300 Ω·cm [34] and therefore the calculated resistance is ~ 22 Ω. In order to simplify the simulation, the measured bare Si sample is represented by 5 µm × 5 µm × 5 µm silicon cube. It is boron-doped with concentration 5×10^{14} cm^{-3}. Tungsten is used as probe with penetration depth T_p (Figure 3.8a) and area $L_p \times L_p$ (Figure 3.8b).

Figure 3.8c shows the simulated $I_P(V_P)$ curves with ohmic (open symbols) and Schottky (solid line) contacts between silicon and chuck. The passage from ohmic to Schottky was obtained by defining electric boundary conditions as Schottky. The Schottky barrier is set by inputting work-function for the probe. The recombination velocities are used by default and no tunneling mechanism is considered. Obviously, the curve best corresponding to our experimental results is the one for ohmic contact between silicon and chuck. Note that this is in perfect agreement with the experimental results, showing that the transport is dominated by the Schottky diode D_1 (probe/silicon).

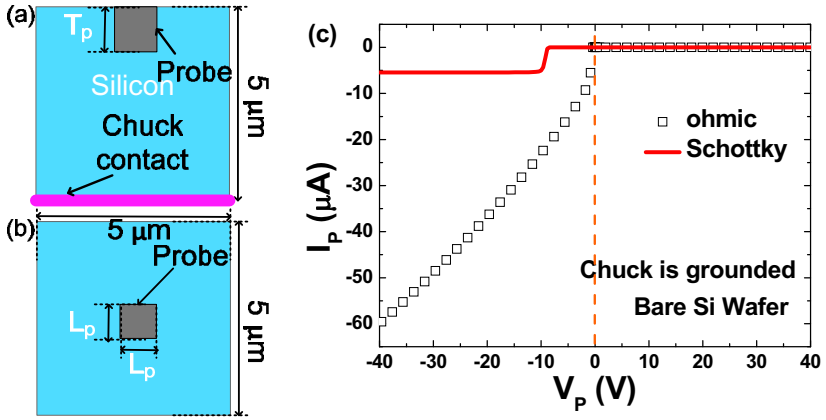

Figure 3.8: *(a) Cross-section, (b) top-view for bare wafers and (c) comparison of simulated $I_P(V_P)$ curves for bare wafers with ohmic and Schottky silicon/chuck contact. The geometry for tungsten probe is: L_P = 100 nm and T_P = 100 nm.*

- **Impact of probe geometry on the simulations**

The geometry of the contact between probe and samples has an important influence on the simulations. Figure 3.9a compares the $I_P(V_P)$ curves with different probe size (L_P). With L_P enlarging, the probe current increases. The area for the cross-section of actual probes is ~ 5×10^{-5} cm^2 (πr^2, $r \sim 40$ µm). Considering that the area of simulated silicon (5 µm × 5 µm) is smaller than the real one (1 cm × 1 cm), we set L_P as 100 nm.

The effect of probe (T_P) penetration depth on the current is given in Figure 3.9b. For deeper probe penetration, the probe current increases. Note that these simulations correspond to the effect of probe pressure on the current in experiments (Figure 3.4a). For silicon-on-insulator, it is assumed that the probe penetrates around 10 nm more deeply when the pressure increases per 10 g [35]. Therefore, 100 nm is chosen for our simulation.

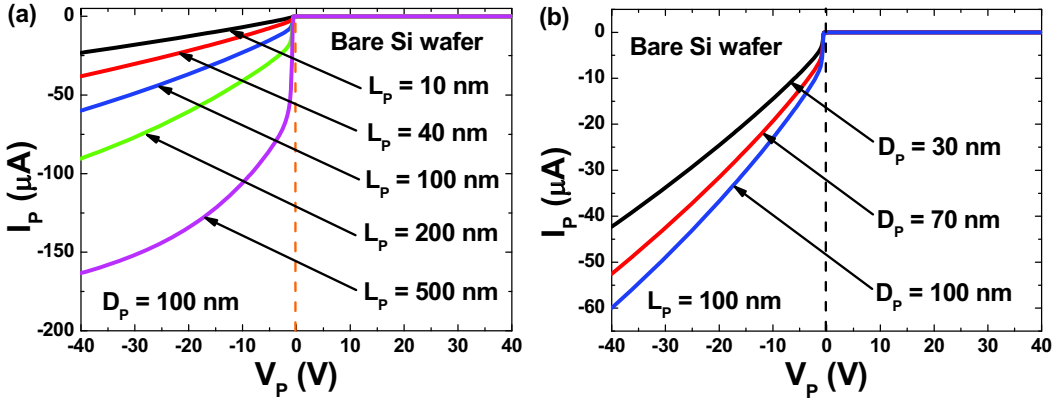

Figure 3.9: *Simulated $I_P(V_P)$ curves with different (a) probe sizes and (b) penetration depth.*

3.2.2 Bonded wafers: Schottky contact and series resistance

The equivalent model of the bonded wafers (cross-section in Figure 3.7) has four Schottky diodes and several resistances associated with the different material layers (Figure 3.10a). Modeling and parameters extraction based on this configuration is not easy to implement. Furthermore, we have demonstrated that the Schottky contact of probe/silicon dominates the $I(V)$ behavior in this configuration for both bare and bonded wafers. Therefore, we regard the other three Schottky contacts as resistors, as shown in Figure 3.10b.

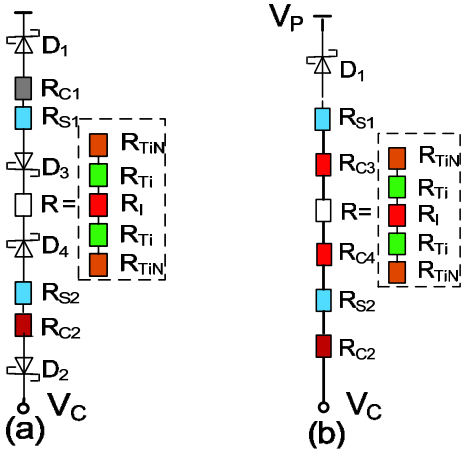

Figure 3.10: *(a) Real model and (b) simplified model for bonded wafers. D_1, D_2, D_3 and D_4 denote the Schottky diodes. R_{C2}, R_{C3} and R_{C4} represent the contact resistances.*

Therefore, the simulation of bonded wafers can be represented by a bare wafer connected to a resistor at the bottom of the Si plate, as shown in Figure 3.11a. The Schottky contact is defined at the tungsten/silicon interface. Figure 3.11b shows the simulated $I(V)$ current for bonded wafers. The probe current (I_P) does not seem to be

influenced by series resistance smaller than 10 kΩ, but decreases for series resistances larger than 10 kΩ. This proves that only a series resistance large enough has a significant effect on the probe current. Based on these simulations, we will validate the extraction method, but before that, we need to express the bases of the model used for the extractions.

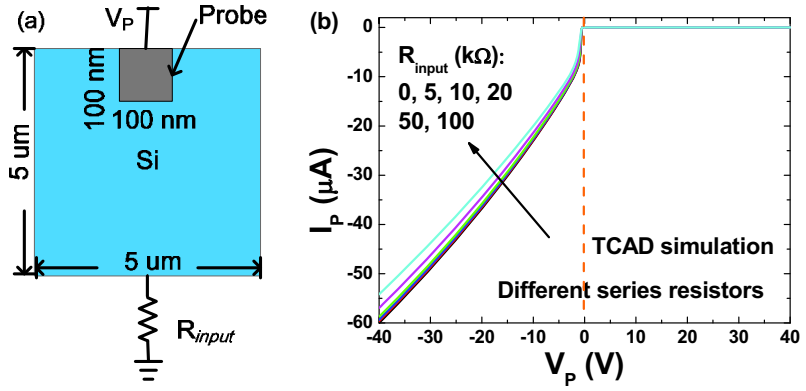

Figure 3.11: *(a) TCAD simulation structure for the bare wafers with a parasitic resistance (R_{input}), representing bonded wafers; (b) simulated $I_P(V_P)$ curves with different input resistors.*

4. Model for estimation of bonded interface

4.1 Estimation principle

TCAD simulations show that a silicon plate connected to a series resistance (Figure 3.11a) can reproduce the $I(V)$ behavior of bonded wafers. The equivalent model is given in Figure 3.12a. When the probe/silicon Schottky diode (D_1) is forward-biased (negative V_P for grounded chuck in Figure 3.4a and Figure 3.6a), the corresponding energy band diagram is given in Figure 3.12b. According to [28], the thermionic emission process would be dominant for forward-biased Schottky diodes in moderately doped semiconductors ($\leq 10^{17}$ cm^{-3}) operated at room temperature. Electrons are emitted from the tungsten probe over the potential barrier into the p-type semiconductor.

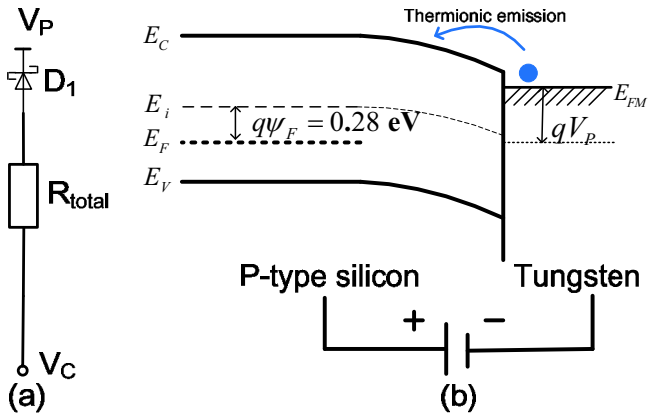

***Figure 3.12**: (a) Our simplified model for bonded wafers and (b) energy band diagram when D_1 is forward-biased. E_F and E_{FM} are the Fermi level for semiconductor and metal. ψ_F is the Fermi potential for p-type silicon.*

We assume that the edge leakage current and interface current due to traps at the metal-semiconductor interface can be neglected. Consequently, the $I(V)$ relationship of a Schottky diode is expressed as [36]:

$$I = I_{Sat}\left(e^{qV/nkT} - 1\right) \tag{3.4}$$

$$I_{Sat} = A_{eff} A^* T^2 e^{-q\phi_B/kT} \tag{3.5}$$

Here, n is the ideality factor, A_{eff} is the effective area, A^* is the Richardson constant ($32\ \mathrm{A\cdot cm^{-2}\cdot K^{-2}}$) and ϕ_B is the barrier height. If $V \gg 3kT/q$, the exponential relationship dominates and Eq. (3.4) can be approximated as [36]:

$$\log I = \log I_{Sat} + \frac{qV}{nKT\ln 10} \tag{3.6}$$

The ideality factor n is obtained from the slope of $\log I(V)$ curves. The intercept yields the reverse bias saturation current I_{Sat} and thus the barrier height can be calculated from Eq. (3.5). Figure 3.13a gives the simulated $\log|I_P|$ ($|V_P|$) curves without and with series resistance. For $|V_P| < \phi_B$, the conventional Schottky model shows good agreement with simulation and $\log|I_P|$ almost superpose for both cases. Table 3-II summaries the extracted parameters for simulations based on the classical Schottky model. The extracted ideality factors approximate theoretical value (~ 1). The barrier height (~ 0.77 eV) is almost independent of R_{input}, close to the theoretical

value (0.62 eV, the work-function for tungsten in the simulation is 4.55 eV). Only for $|V_P| > \phi_B$ does the series resistance have a significant effect on the current. With the series resistance rising, the probe current decreases.

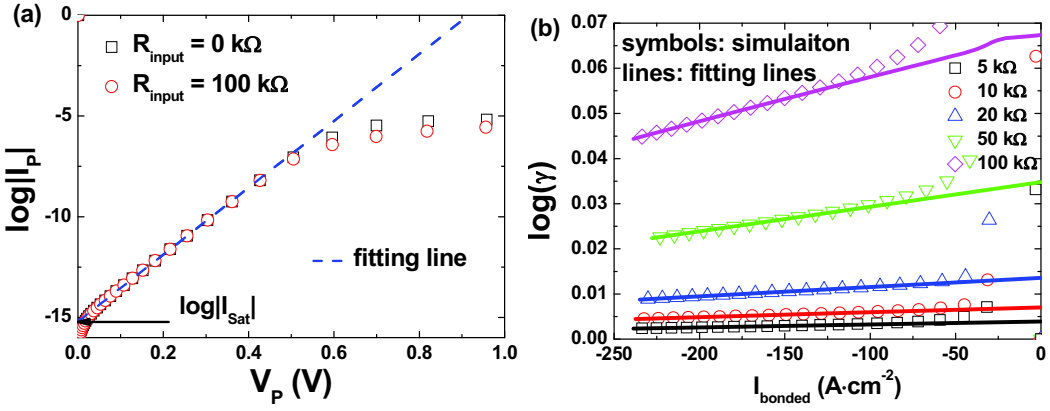

Figure 3.13: (a) *Simulated log|I_P|(|V_P|) curves with different input resistors and (b) log(t) versus I_{bonded}.*

Table 3-II: *Extracted parameters from simulations.*

R_{input} (kΩ)	n	ϕ_B (V)	R_{eff} (kΩ)
0 Ω	1.05	0.77	
5 kΩ	1.01	0.77	1.9
10 kΩ	1.01	0.77	3.2
20 kΩ	1.01	0.77	6
50 kΩ	1.01	0.77	16
100 kΩ	1	0.77	31

For large $|V_P|$, the voltage drop across the series resistance (R_{total}) is large enough to be considered, so Eq. (3.6) must be rewritten as [37]:

$$\log I_{bonded} = \log I_{Sat} + \frac{q(V - I_{bonded}R_{eff})}{nkT\ln 10} \tag{3.7}$$

where R_{eff} is an effective supplementary resistance used for estimating the quality of the bonding interface (not the real series resistance). I_{Sat} for bare wafers with and without series resistance are almost at the same order of magnitude (10^{-9} A). Thus, substituting Eq. (3.6) into Eq (3.7), we have:

$$R_{eff} = \frac{\log(\gamma)}{\alpha I_{bonded}} \tag{3.8}$$

where $\gamma = I_{bare}/I_{bonded}$ and $\alpha = q/nkTln10$. Eq. (3.8) shows a linear dependence of $log(\gamma)$. In Figure 3.13b, we plot $log(\gamma)$ versus I_{bonded}, which is indeed linear The slope yields the effective resistance, which is given in Table 3-II. The extracted R_{eff} are almost equal to 1/3 of the input values for simulations ($R_{input}/R_{eff} \approx 3$). Nevertheless, R_{eff} can still be used to represent the variation of series resistance, which mainly results from the resistance of bonding interface in the experiments. In next sub-section, we will apply this estimation method to experimental data.

4.2 Experimental results

As demonstrated in the previous sections, all the experiments clearly showed that the $I(V)$ behavior in the bonded wafers is dominated by the Probe/Silicon Schottky diode (D_1). Therefore, the other interfaces and materials can be modeled as resistances, as shown in Figure 3.10b. TCAD simulations also demonstrated that only large series resistance can significantly vary the probe current. What is the resistance that has the strongest impact here? The resistances for different material layers calculated from Eq. (3.3) are detailed in Table 3-III. It is clearly seen that resistances for silicon, TiN and Ti layers are too small to affect the probe current. TiN/p-type silicon has been reported to be a good ohmic contact due to the interdiffusion between Si/TiN layers [38], [39]. Therefore, the contact resistance of Si/TiN (R_{C3} and R_{C4}) can be neglected. According to [37], the contact resistance for a Cu/Si Schottky diode is ~ 17 Ω. Consequently, it is likely that the series resistance mainly results from the bonding interface and therefore Figure 3.10b is further simplified as Figure 3.12a.

Table 3-III: *Calculated resistances for different material layers ($S = 1\ cm^2$).*

Material layer name	Resistivity (Ω·cm)	Thickness (nm)	Resistance (Ω)
Si	300	7.25×10^5	22 (R_{S1} or R_{S2})
TiN	7×10^{-5}	60	4.2×10^{-10} (R_{TiN})
Ti	1.5×10^{-4} [40]	10	1.5×10^{-10} (R_{Ti})
		5	0.75×10^{-10} (R_{Ti})

For small $|V_P|$, the conventional Schottky model still works, as shown in Figure 3.14. All the extracted ideality factors are close to 1. The extracted barrier heights are

around 0.95 eV, higher than the calculated value (0.62 eV). This can be explained by our use of mean value of work-function for tungsten to calculate the theoretical barrier height. In fact, the work-function for tungsten can vary from 4.18 V to 5.25 V depending on crystallographic directions and experimental methods [29].

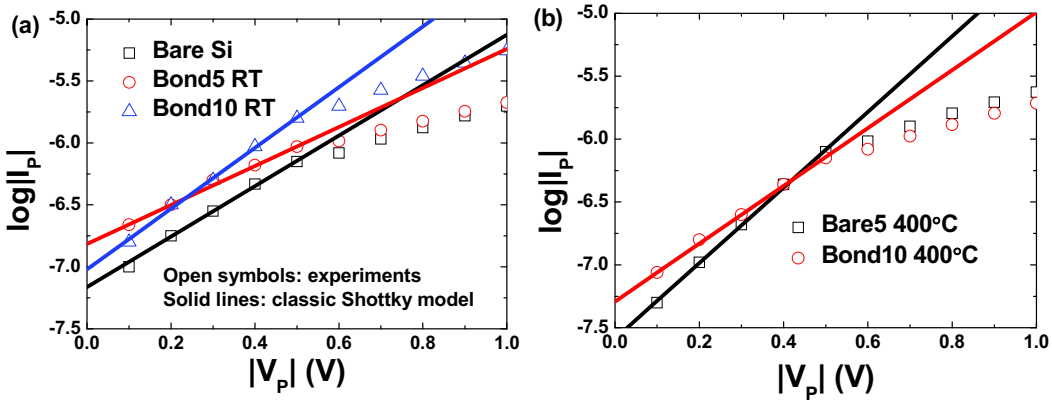

Figure 3.14: *Application of classic Schottky diode equation under small $|V_P|$ bias for wafers (a) without and (b) with annealing.*

Table 3-IV: *Extracted parameters from experiments.*

			n	ϕ_B (V)	R_{eff} (kΩ)
Experiments	**Bare Si**		1	0.93	
	Bond5	**RT**	0.91	0.92	11
		400°C	1.03	0.94	6.3
	Bond10	**RT**	0.89	1	16
		400°C	0.82	0.95	10

For larger $|V_P|$, the effect of series resistance must be considered and therefore the adapted Schottky diode model is used (Eq. (3.7)), as shown in Figure 3.15. Both bonded wafers exhibit larger R_{eff} before annealing (Table 3-IV). After 400°C annealing for two hours, R_{eff} decreases. This is consistent with the fact that annealing improves the quality of bonding interface and therefore reduces the series resistance.

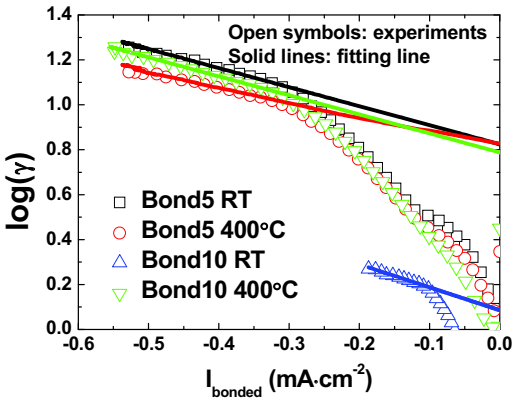

Figure 3.15: *log(γ) versus I_{bonded} for bonded wafers under large $|V_P|$ bias.*

5. Chapter summary

In this chapter, we have shown a simple method for estimating the bonding quality of metal-bonded wafers by $I(V)$ measurements. The conventional Schottky $I(V)$ equation used only for smaller applied voltage has been adapted by taking into account the large bonding resistance. TCAD simulations and $I(V)$ experiments prove the feasibility of this estimation method for bonded wafers. The extracted bonding resistance decreases after annealing, which is consistent with the technological improvement of the interface by annealing process.

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Chapter 4: Parasitic bipolar effect in ultra-thin FD SOI MOSFETs

Planar FD SOI transistors are one compelling solution to reduce SCEs due to excellent electrostatic control in the channel [1]–[3]. Benefitting from this, a 6T Static Random-Access Memory bit-cell with small area (~ 0.176 μm^2) and low leakage (~ 6.6 pA/μm) has been achieved by C. Fenouillet-Beranger *et al.* in 32 nm node [4]. Recently, D. Jacquet *et al.* [5] have demonstrated a 3 GHz dual core processor in 28 nm planar Ultra-Thin BOX and Body (UTBB) fully-depleted CMOS technology CMOS with ultra-wide voltage range (0.52 V to 1.37 V on supply and 0 to 1.3 V forward body bias voltage) and energy efficiency optimization. In addition, multiple threshold voltage tuned by back-gate has been used to improve the robustness of clock tree in 28 nm planar UTBB FD SOI technology [6]. A critical aspect in advanced MOSFETs is the drain leakage, especially when amplified by the parasitic bipolar transistor [7].

In this chapter, we focus on leakage currents and parasitic bipolar transistor (PBT) in ultra-thin FD SOI devices (≤ 10nm), especially the drain leakage amplified by parasitic bipolar transistor (PBT). We will show through experiments and simulations that a bipolar amplification is present even in ultra-thin short-channel devices, being caused by the holes generated via band-to-band tunneling. Section 1 makes an introduction about the various contributions to drain leakage. Section 2 gives evidence of parasitic bipolar effect through experiments and explains its origin through simulations. In Section 3, we will discuss the effect of back-gate on parasitic bipolar effect. In section 4, two methods for the extraction of bipolar gain β are proposed, validated through simulations and applied to our experiments.

1. Contributions to drain leakage

With the increasing MOSFET performance requirements and particularly the power consumption reduction, several goals are being pursued: high ON current (I_{ON}), low OFF current (I_{OFF}) and small subthreshold swing [8]–[10]. In order to obtain a high I_{ON}/I_{OFF} ratio, special attention has to be devoted to the leakage mechanisms that increase I_{OFF}. Figure 4.1a shows the main OFF leakage contributions for a short-channel FD SOI MOSFET (n-channel):

- Subthreshold conduction I_{sub} [11];
- Direct gate tunneling (I_{FG}), including gate-to-source tunneling current I_{GS}, gate-to-channel tunneling current I_{GC} and gate-to-drain tunneling current I_{GD} [12];

— Impact ionization (II), including electron flow I_{e_II} and hole flow I_{h_II} [13];

— Band-to-band tunneling (BTBT), including electron flow I_{e_BTBT} and hole flow I_{h_BTBT} [13], [14];

— Parasitic bipolar transistor (PBT), induced by II or BTBT [15], [16].

Depending on the polarization conditions, the OFF-state current I_{OFF} has different contributions (Figure 4.1b).

① For V_{FG} = 0 V and small V_D (*e.g.* 0.1 V), the OFF-state current only contains the subthreshold conduction and gate tunneling current ($I_{OFF} = I_{sub}+I_{FG}$).

② If the drain is biased at high voltage (*e.g.* 1.5 V), the drain leakage induced by impact ionization will be added ($I_{OFF} = I_{sub}+I_{FG}+I_{e\_II}$).

③ For V_{FG} negative enough (*e.g.* -0.5 V) and small $V_{D,}$ the OFF-state current mainly contains BTBT and direct gate tunneling currents ($I_{OFF} = I_{e\_BTBT}+I_{FG}$).

④ For V_{FG} negative enough (*e.g.* −0.5 V) and large $V_{D,}$ II current and the leakage amplified by PBT will be added to BTBT and direct gate tunneling currents ($I_{OFF} = I_{e\_BTBT}+I_{FG}+I_{e\_II}+I_{PBT}$).

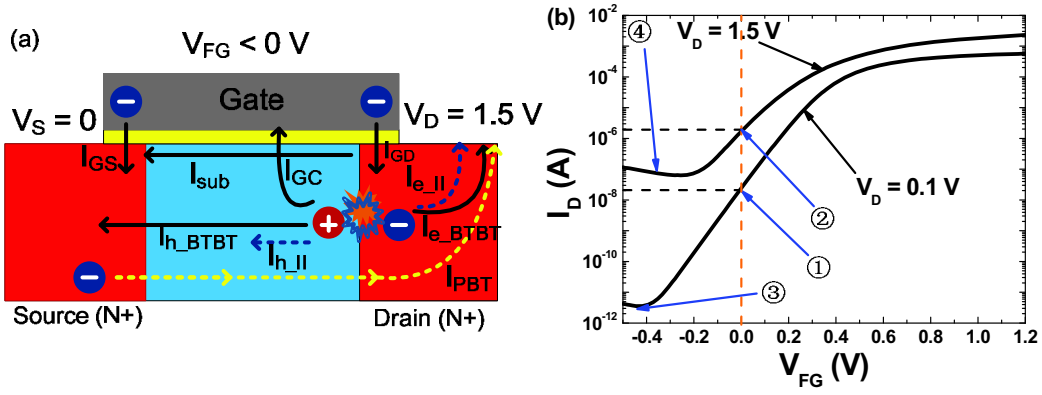

Figure 4.1: *(a) Schematic of all the leakage flows for a short-channel FD SOI MOSFET (n-channel) and (b) comparison of drain currents measured at high and low drain bias.*

1.1 Conventional drain leakage

- **Subthreshold conduction**

When the front-gate voltage is biased below threshold voltage (V_T) weak inversion conduction between drain and source occurs, leading to the subthreshold current I_{sub}. This corresponds to the linear region of the drain current in the semi-logarithmic plot of I_D versus V_{FG} (see Figure 4.1b). Unlike the strong inversion region where the drift

current dominates (V_{FG} > 0.4 V in Figure 4.1b), the subthreshold conduction is governed by the diffusion mechanism and the drift component is negligible [11]. According to [17], the subthreshold current for SOI devices can be expressed:

$$I_{sub} \propto exp\left(\frac{V_{FG} - V_S}{n_{sub}\upsilon_T}\right) \tag{4.1}$$

Here, υ_T is the thermal voltage ($\upsilon_T = kT/q$) and n_{sub} is the subthreshold slope factor. For a long-channel uniformly-doped device with thick film it can be calculated:

$$n_{sub} = \frac{C_{GC} + C_P}{C_{GC}} \tag{4.2}$$

where C_{GC} is the unit coupling capacitance between gate and channel and C_P denotes all other capacitances (interface traps and depletion region). For small drain voltage, C_{GC} and C_P can be determined according to the depletion, accumulation and inversion at the Film/BOX interface. When the gate length is scaled down, the subthreshold slope factor degrades and therefore the subthreshold conduction current is enhanced in the short-channel device [18]. On the other hand, the coupling effect in ultra-thin FD SOI MOSFET becomes more significant and the calculations of subthreshold slope factor is more complicated [19].

- **Direct gate tunneling**

With the device size down-scaling, extremely thin gate oxides are imperative and therefore the leakage current that directly tunnels through the gate oxide becomes more and more significant [20]. It was reported that the gate leakage current is comparable to the subthreshold current for devices with EOT = 1.4 nm and effective gate length 22 nm [21]. This direct tunneling gate current cannot only lead to the failure of the circuit functionality, but also increases the standby power consumption. On the other hand, the introduction of high-k materials results in a thin interfacial layer formed by SiO_x or a mixed oxide between silicon and the high-k materials [22], [23]. The traps generated by high-k materials can assist the electrons tunneling through the stacked layers [24]–[27].

Figure 4.1a shows the three main gate tunneling currents: I_{GD}, I_{GS} and I_{GC} for an n-channel MOSFET in the region of concern here (V_S = 0 V, V_D > 0 V, V_{BG} = 0 V and

V_{FG} < 0 V). When the front-gate voltage is negative, the holes in the film will tunnel through the gate oxide as I_{GC}. Meanwhile electrons from the gate will tunnel through the gate oxide overlapping drain and source as I_{GD} and I_{GS}. If the drain voltage rises, I_{GD} increases. Usually, I_{GC} is much smaller than I_{GD} due to the large tunneling mass of holes [21]. Therefore, I_{GD} dominates the gate current.

- **Impact Ionization**

Basically, impact ionization is a generation process involving at least three particles. Carriers can gain energies high enough while traveling through high field regions, and then undergo scattering events with bonded electrons in the valence band. The excess energy is transferred to this electron lifted into the conduction band, which results in the creation of a new electron-hole pair. This secondary electron-hole pair can also have a rather high energy to trigger another collision. Thus, the carrier density increases rapidly in an avalanche generation process. Figure 4.2 sketches this effect for pure electron induced generation.

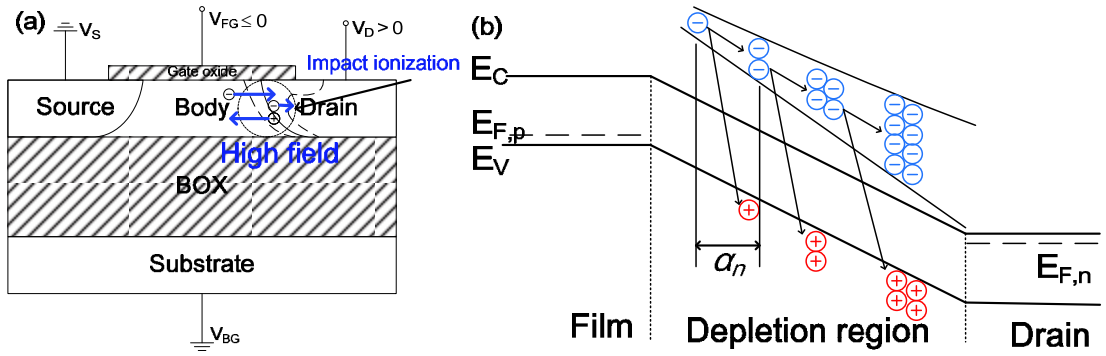

Figure 4.2: *(a) Schematic of impact ionization in a SOI MOSFET and (b) symbolized process of impact-ionization avalanche generation induced by a pure electron. After an electron is accelerated along an average distance α_n, it undergoes a collision, leading to the generation of a new electron-hole pair due to the excess energy. Consecutive collisions can trigger an avalanche. $E_{F,p}$ and $E_{F,n}$ are respectively the quasi Fermi level in the film and drain [28].*

The $I(V)$ behavior of a transistor is heavily affected by impact ionization. In MOS devices, impact ionization mainly happens in the channel near the drain (Figure 4.2a). For reverse-biased p-n junctions (body-drain), the avalanche breakdown usually determines the maximum breakdown voltage. In order to overcome this, doping engineering of drain such as lightly-doped drain (LDD) have been adopted to reduce the maximum field for a given voltage.

- **Band-to-band tunneling**

Band-to-band tunneling happens in the gate-drain overlap region (see in Figure 4.3a) [29]. When gate is biased negatively, the energy band at point P will bend as shown in Figure 4.3b. Electrons in the inverted overlap region (N^- Drain, LDD) tunnel across the Si band gap (as potential barrier) into the quasi-neutral drain (energy band does not bend) and the remained holes in the valence band flow freely into the body due to the lateral electric filed. Depending on the positions of two extrema where band-to-band tunneling happens in *k*-space, there are two kinds of physical mechanisms: "direct" band-to-band tunneling (the two extrema locate at the same point) and "indirect" band-to-band tunneling (the two extrema do not locate at the same point) [30].

— For "**direct" band-to-band tunneling**, an electron directly tunnels through the energy gap without the absorption or emission of a phonon. The "direct" tunneling process is negligible in silicon because the transmission probability decreases rapidly with increasing barrier height [29], [31].

— For "**indirect" band-to-band tunneling**, a tunneling electron or hole acquires a change in momentum by absorbing or emitting a phonon in order to keep the momentum and energy balanced. "Indirect" tunneling is the main tunneling process in indirect band gap semiconductors, such as silicon, unless the gate dielectric is very thin.

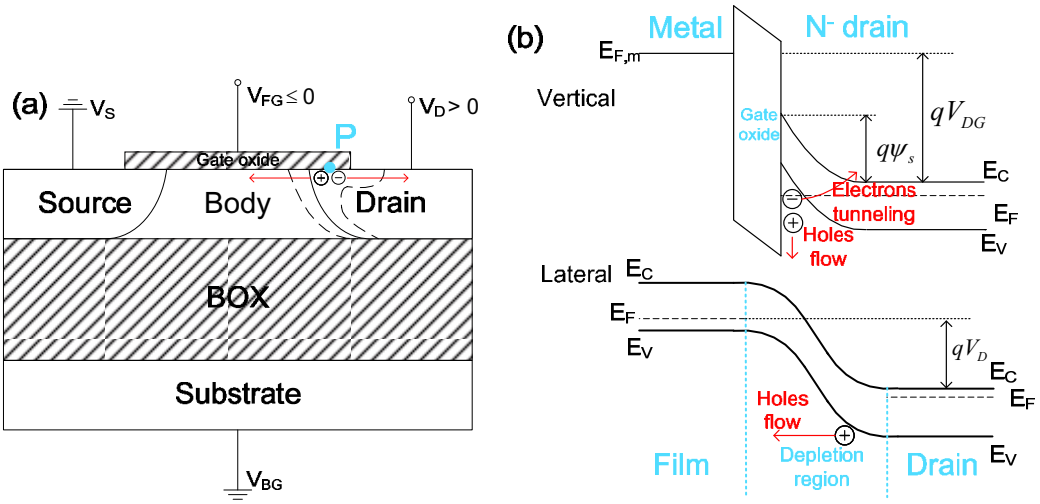

Figure 4.3: *(a) Schematic of band-to-band tunneling and (b) vertical and lateral energy bands at point P [32].*

The "indirect" tunneling current is usually modeled using the Wentzel-Kramers-Brillouin approximation [30]:

$$J = A \cdot E_{max}^2 \cdot exp\left(\frac{-B}{E_{max}}\right) \tag{4.3}$$

The prefactor A and exponential factor B are tunneling parameters, depending on the bandgap and carrier effective mass in the channel material. E_{max} is the critical electrical filed. Since E_{max} is proportional to gate voltage, the BTBT current is independent on the gate length. This model is widely used to predict the BTBT current [14], [31], [33]. However, this model has several weaknesses [34]:

a) The critical electric field cannot be determined for small devices since the electric field is not uniform.
b) Both tunneling parameters (A and B) require calibration for any new structure/material.
c) A nonzero generation rate cannot be obtained even at equilibrium (because A $\neq$ 0 and B $\neq$ 0).
d) The same generation rate for electrons and holes is not true due to the difference of tunneling mass between electrons and holes.

Recently, a dynamic non-local model is proposed [35]. It is applicable to arbitrary tunneling barriers involving nonuniform electric field (especially in short-channel devices) [33], [36]. Tunneling paths are dynamically determined according to the gradient of the band energy. This model accounts for both direct and phonon-assisted tunneling process, which has been widely used in the literatures to predict the performance of tunneling FETs [37], [38].

To all these mechanisms, we should add amplification due to the parasitic bipolar effect [16], which is very important in short-channel transistors.

1.2 Parasitic bipolar amplification

The parasitic bipolar effect was firstly invoked by E. Sun *et al.* to explain the latch-up breakdown in bulk MOSFETs [39]. In SOI MOSFETs, the drain and source work as collector and emitter of the parasitic bipolar transistor (n^+-p-n^+), whereas the floating body is regarded as the base, as shown in Figure 4.4. As opposed to the conventional

bipolar transistor, the PBT in SOI MOSFETs does not have a base contact (floating body). Nevertheless, when the front-gate is negative and the drain is positive, holes are generated either by BTBT or II on the drain side and they are driven into body by the lateral electric filed. The body potential increases and turns on the source-body junction (here, playing the role of base-emitter junction); consequently electrons are injected from source and collected by the drain as collector current I_C.

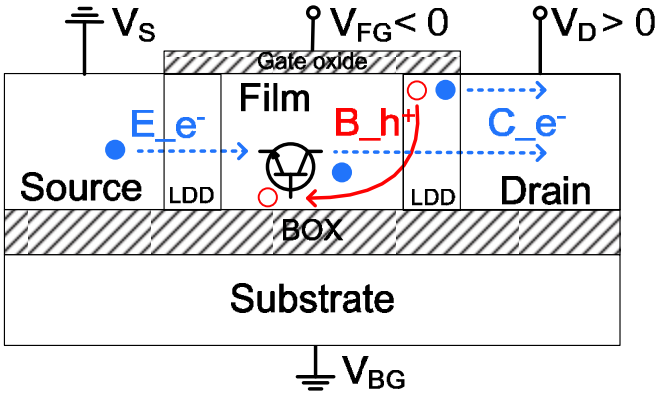

Figure 4.4: *Schematic cross section for an n-channel fully-depleted MOSFET when PBT happens. B_h$^+$, C_e$^-$ and E_e$^-$ are respectively the flows of carriers at base, collector and emitter.*

Several groups have studied the parasitic bipolar effect, mostly in PD SOI or thick FD SOI devices. Muller *et al.* found that PBT in bulk MOSFETs is mainly induced by II in the high field region [40]. Choi *et al.* simulated the floating-body bipolar effect triggered by II in thick FD SOI MOSFETs [15]. Ploeg *et al.* modeled the current gain for II-induced parasitic bipolar effect in thick SOI MOSFETs [41]. Experimental results for partially depleted SOI MOSFETs operated at high temperature were reported by Reichert *et al.* [42]. In addition, Chen *et al.* proved that BTBT could also trigger the bipolar effect, leading to the enhancement of gate-induced drain leakage in short-channel MOSFETs fabricated on thick SOI films [16]. There are two key elements in these studies: (a) the dominated mechanism generating holes that accumulate at the body and (b) the thickness of the body. All the research involves the partially-depleted SOI or very thick FD SOI devices. Recently, Fenouillet-Beranger *et al.* noted a PBT in ultra-thin FD SOI MOSFETs [43]. In next section, we will show the experimental and TCAD simulation evidences of parasitic bipolar effect in ultra-thin FD SOI MOSFETs.

2. Evidence of parasitic bipolar effect in ultra-thin FD SOI MOSFETs

2.1 Experimental results

2.1.1 Device structure

The structures used are n-channel FD SOI MOSFETs from CEA-Leti and STMicroelectronics, schematically shown in Figure 4.5. The measured samples are detailed in Table 4-I. The effective thickness of stacked gate insulator is 1.6 nm. High-k dielectric material and metal gate technology are adopted. The BOX thickness is 25 nm. The lengths of spacer and overlap region are 5 nm and 2 nm, respectively. The film is low p-type doped (N_{film} = 10^{15} cm^{-3}). The heavily and lightly-doped source/drain concentrations (HDD and LDD) are 10^{20} cm^{-3} and 3 × 10^{19} cm^{-3}, respectively. The gate length varies between 30 nm and 1000 nm.

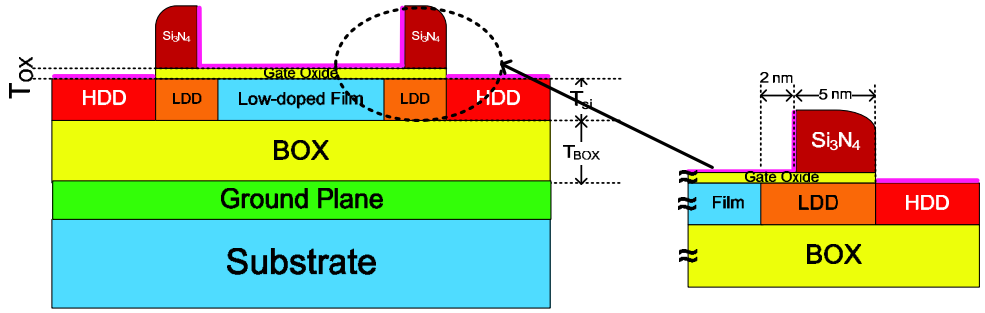

Figure 4.5: *Schematic view of the FD SOI MOSFET used for the experiments and simulations.*

Table 4-I: *Parameters for measured FD SOI MOSFETs.*

Parameter	Acronym (Units)	Value
Film thickness	T_{si} (nm)	10, 7, 5
Gate oxide thickness	EOT (nm)	1.6
BOX thickness	T_{BOX} (nm)	25
Film doping	N_{film} (cm^{-3})	10^{15}
LDD doping	N_{LDD} (cm^{-3})	3 × 10^{19}
Gate length	L_G (nm)	30 ~ 1000

2.1.2 Experimental evidence of enhanced leakage current

$I(V)$ measurements were carried out using Agilent 4156B Semiconductor Parameter Analyzer. Figure 4.6 compares the transfer characteristics of FD SOI devices for long-channel (Figure 4.6a) and short-channel (Figure 4.6b) devices with 10 nm thick Si-body. In long devices, the drain leakage current (for $V_{FG} < 0$) increases gradually with

V_D. In short-channel device, the behavior is similar only at low bias ($0 < V_D < 1$ V). For higher bias, the drain leakage increase with V_D is clearly sharper and dramatically degrades the transistor OFF-state characteristics. In order to reduce the drain leakage, we need to understand the origin of this sudden amplification occurring for high V_D in short-channel transistors.

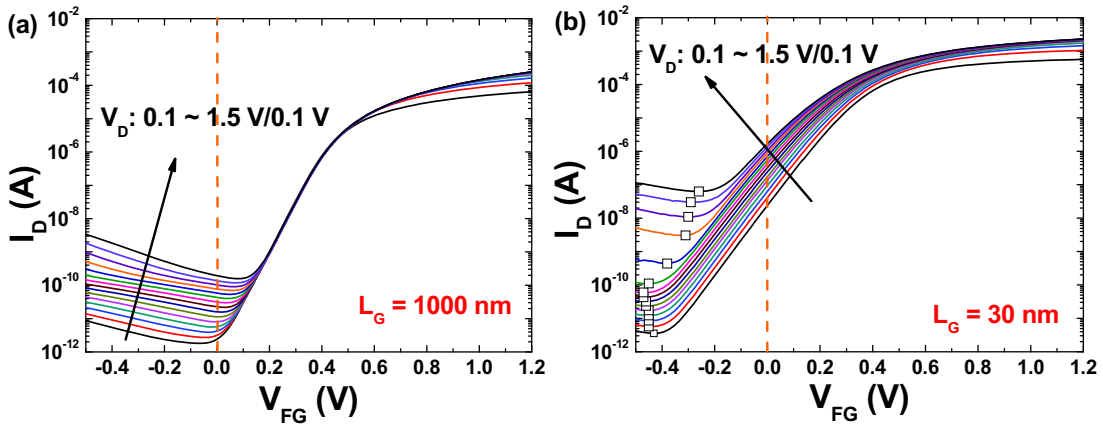

Figure 4.6: *Experimental current versus front-gate bias characteristics of FD SOI NMOS with 10 nm film thickness and different channel length: (a) L_G = 1000 mm and (b) L_G = 30 nm. T_{si} = 10 nm, W = 2000 nm and V_{BG} = 0 V.*

The currents for drain, source, front-gate and back-gate at $V_{FG} = -0.5$ V for long-channel (Figure 4.7a) and short-channel (Figure 4.7b) devices are compared:

— For long-channel devices, the source current I_S remains small when V_D is swept from 0.1 V to 1.5 V. The drain current I_D is dominated by the front-gate current I_{FG} which explains the difference between I_S and I_D. The back-gate current I_{BG} is firstly equivalent to I_{FG} ($V_D < 0.6$ V) and then decreases ($V_D >$ 0.6 V). The order of magnitude for I_{BG} is always smaller than 10^{-10} A.

— For short-channel devices, I_{FG} only dominates the leakage when $V_D < 1$ V (Figure 4.7b); for higher V_D, I_D and I_S become equal and they are far larger than I_{FG}. This increase in leakage current reveals a different mechanism turned on at high V_D. Note that the back-gate current I_{BG} can always be neglected (~ 10^{-11} A).

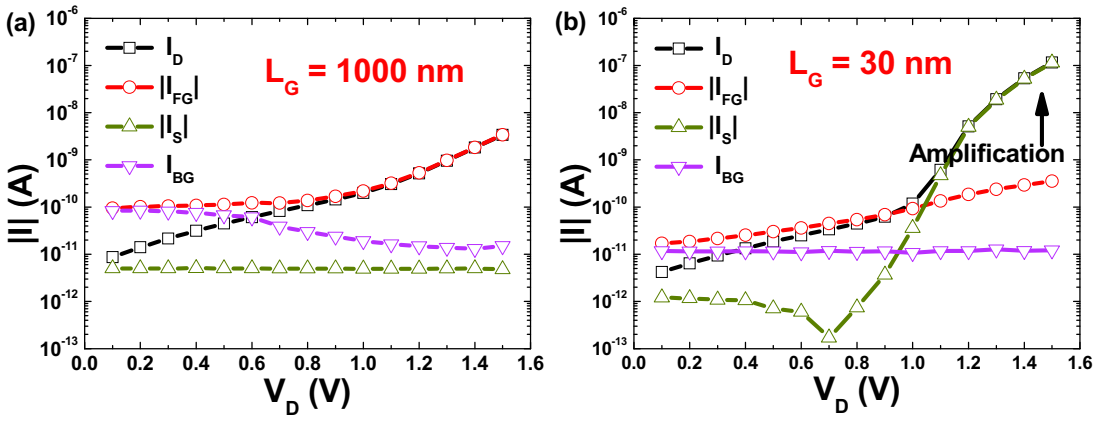

Figure 4.7: *Comparison of drain, source, front-gate, and back-gate currents at V_{FG} = −0.5 V for: (a) L_G = 1000 nm and (b) L_G = 30 nm FD SOI MOSFETs.*

Two conclusions can be obtained from the comparisons of drain, source, front-gate and back-gate between long- and short-channel devices:

— The front-gate current governs the leakage of long-channel device.

— The current amplification observed in short-channel devices can be associated with an activation of the parasitic bipolar transistor, which indeed needs short base to manifest itself (L_G < 100 nm).

Siince the film behaves as the base of the parasitic bipolar by accumulating holes, as we described previously, the thickness of the film is expected to play an important role in the parasitic bipolar effect. Next, we will evidence the correctness of the assumption of PBT by measuring the short-channel devices with different film thickness. Figure 4.8 reports the experiments on short MOSFETs (L_G = 30 nm) with variable film thickness. For V_D = 1.2 V, 10 nm thick devices exhibit current amplification (Figure 4.8a). However, if the body is thinned down to 7 nm and 5 nm, this amplification is suppressed ($I_D \approx I_{FG}$). When V_D is increased from 1.2 V up to 1.5 V (Figure 4.8b), the bipolar amplification becomes stronger for T_{si} = 10 nm and starts to also appear in 7 nm thick MOSFET. This indicates that increasing V_D can turn on the PBT even in thinner films. Note that no bipolar effect is observed for T_{si} = 5 nm. Higher V_D, which should trigger the PBT in 5 nm film, cannot be applied due to the breakdown of gate oxide. The impact of film thickness is related to the effective carrier lifetime. It is known that in thinner films the lifetime is shorter due to the increased contribution of the front and back interfaces [44]–[46]. A short lifetime weakens the gain of the bipolar transistor.

Until here, we have shown the experimental evidence of PBT in ultra-thin FD SOI MOSFETs; in the next section, we will verify through simulations the origin of the leakage current amplification.

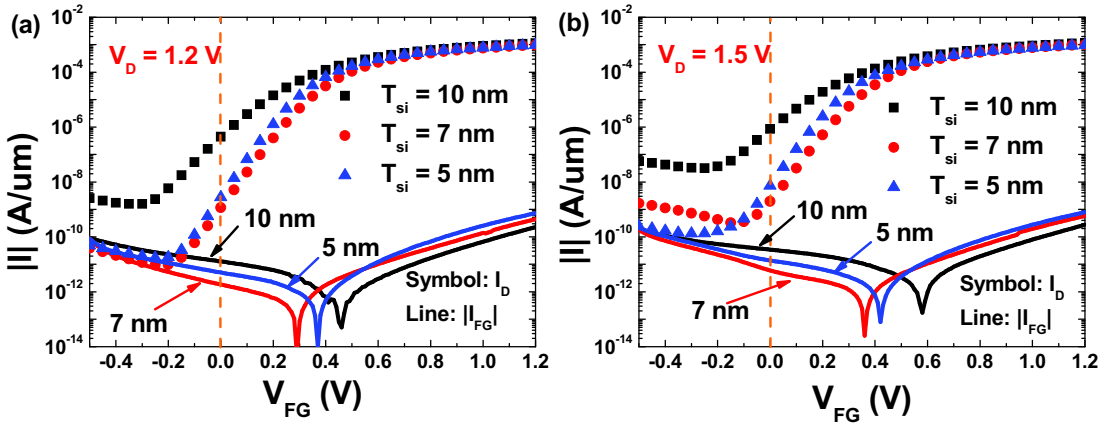

Figure 4.8: *Current versus front-gate bias $I_D(V_{FG})$ characteristics measured in short MOSFETs (L_G = 30 nm) with different Si-body thicknesses: (a) V_D = 1.2 V and (b) V_D = 1.5 V.*

2.2 Simulations

Though we have experimentally demonstrated the PBT in ultra-thin FD SOI MOSFETs, there are still two questions:

- Which mechanism provides the holes as base current: band-to-band tunneling current or impact ionization current?
- How does the geometry of devices affect the current amplification?

In order to find these answers, two-dimensional simulations are used to reproduce the experimental curves, to confirm that the leakage current amplification is due to the PBT action and to show the origin of the holes flowing in the PBT.

2.2.1 Simulation set up

The simulations were performed with Synopsys Sentaurus TCAD [35]. In order to assess the dominant mechanism, simulations were carried out by activating or not the BTBT and II generation. The structure used in the simulations mimics the experimental devices (Figure 4.5), featuring undoped body (N_A = 10^{15} cm^{-3}), source/drain concentrations of 10^{20} cm^{-3} and LDD regions of 3 × 10^{19} cm^{-3}. Fermi–Dirac statistics was employed. All the implanted regions have a constant doping profile. The mobility model used in the simulations includes the effects of doping,

electric field and velocity saturation. For BTBT, the dynamic non-local tunneling model was used, which is applicable to arbitrary tunneling barriers involving nonuniform electric field (especially in short-channel devices). Tunneling paths are dynamically determined according to the gradient of the band energy. This model accounts for the direct and phonon-assisted tunneling process, which is widely used in the literature to predict the performance of tunneling FETs. The impact ionization was simulated with the accurate temperature-dependent model [47], [48]. In addition, Schokley-Read-Hall and Auger recombination models were included. For sake of clarity, the effect of gate tunneling has not been considered in any simulation. In order to take into account properly the floating body effects, we used the 'transient' option during the voltage ramping.

2.2.2 Origin of the enhanced leakage current

As previously mentioned in the experiments, the presence of holes in the body is the starting point of the parasitic bipolar transistor. They can be provided by band-to-band tunneling and/or by impact ionization which can play a significant role in our FD SOI devices. Here, we want to determine which one triggers the parasitic bipolar effect from simulations. Our simulations are performed considering different phenomena:

- Without BTBT and II
- Only II
- Only BTBT
- With BTBT and II

The $I_D(V_{FG})$ (at V_D = 1.5 V, Figure 4.9a) and $I_D(V_D)$ (at V_{FG} = −0.5 V, Figure 4.9b) curves were simulated taking into account different phenomena. When both BTBT and II are off (dotted lines), the drain leakage is small (~ 1 pA). If II is turned on (circle symbols), I_D does not show any significant difference from the one with both models off, suggesting that II can be neglected even for our highest V_D (1.5 V). If only BTBT is switched on (square symbols), an obvious current amplification is observed. Finally, when both BTBT and II are added (solid lines), the simulated I_D fully overlaps the one with only BTBT. The effect of II can be neglected in this range of V_D. This is in agreement with previous results showing that a higher V_D range is needed

for impact ionization [43]. The conclusion is that the PBT amplification observed when V_D increases from 0.1 V to 1.5 V is induced mainly by BTBT.

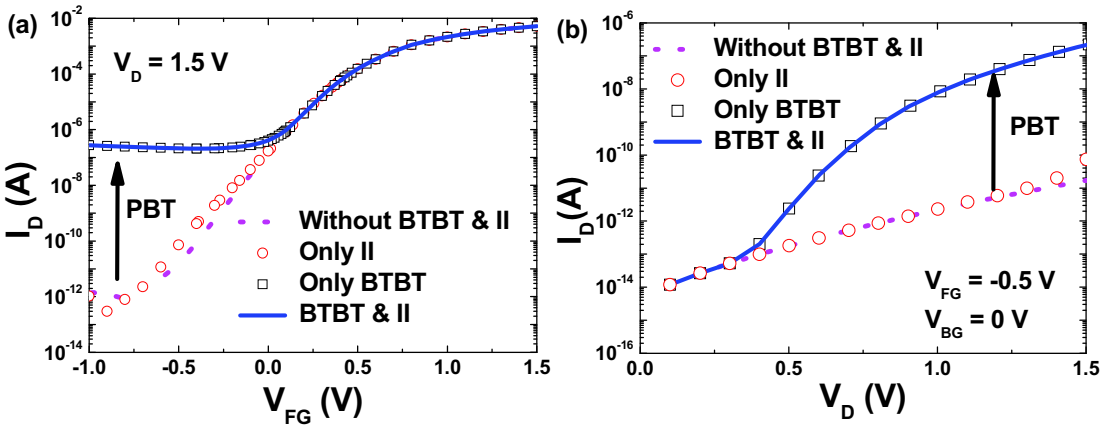

Figure 4.9: *Simulated characteristics for short-channel devices: (a) $I_D(V_{FG})$ and (b) $I_D(V_D)$ at V_{FG} = −0.5 V. T_{si} = 10 nm, L_G = 30 nm and V_{BG} = 0 V.*

In order to understand how BTBT triggers the parasitic bipolar effect in ultra-thin FD SOI MOSFETs, we show the simulated energy band with BTBT on and off. When the front-gate is negatively biased (here, V_{FG} = −0.5 V), the energy band for N^- LDD around drain would be bended as in Figure 4.10a, allowing the electrons in the valence band to tunnel across the energy gap and reach conductance band. The remained holes would flow into the body due to lateral electric field (Figure 4.10b). With BTBT off, this tunneling process is forbidden although the energy band is still bended.

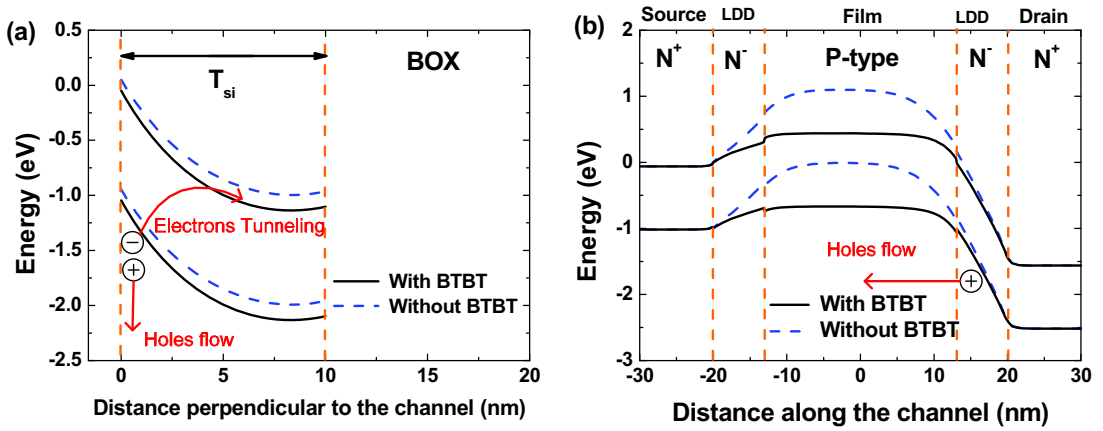

Figure 4.10: *(a) Vertical band diagram at the point of maximum tunneling rate (5 nm away from the drain and into the channel) and (b) band diagram in the lateral direction. T_{si} = 10 nm, L_G = 30 nm, V_{FG} = −0.5 V and V_{BG} = 0 V.*

Figure 4.11a compares the hole profiles with BTBT on and off. Since the holes generated by BTBT flow into the body, the density of holes at the bottom of body with BTBT on is higher than that without BTBT. This will lead to the increase of body potential (Figure 4.11b). In addition, a drain bias large enough (critical V_D) is needed to lower the potential barrier of the body-source junction. With small V_D, the increment of body potential is not large enough and the potential barrier between source and body is still high (Figure 4.11b for V_D = 0.2 V).

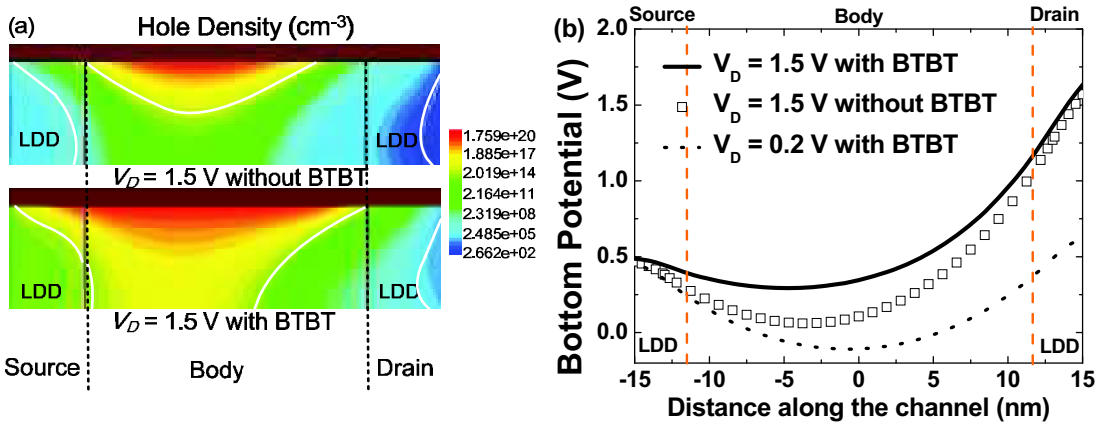

Figure 4.11: *(a) Simulated hole densities and (b) potential profiles at the bottom of the body. The source and drain respectively lie on the left and right side. T_{si} = 10 nm, L_G = 30 nm, V_{FG} = −0.5 V and V_{BG} = 0 V.*

In order to find the critical V_D to activate PBT, three types of simulations were performed:

(i) BTBT model is turned off;

(ii) BTBT is enabled but hole continuity equations are removed: no current associates to holes;

(iii) With the BTBT model on, both electron and hole continuity equations are used.

The corresponding $I_D(V_{FG})$ curves are shown in Figure 4.12. When V_D is low, no leakage amplification is observed (as in the experiments) because the PBT is always off. Thus, all these three model combinations yield superposed curves (Figure 4.12a). With V_D = 1.5 V (Figure 4.12b), the drain leakage without BTBT is the intrinsic current for a MOSFET (I_{MOS}). For case (ii), the drain collects I_{MOS} (unchanged) and also the electrons generated by BTBT; the drain leakage corresponds roughly to the

BTBT current (much larger than the intrinsic current I_{MOS}). The current amplification occurs in case (iii) due to the addition of hole continuity equation. The hole current acts as base current and turns on the PBT. The electron current densities in the horizontal direction, for V_D = 1.5 V and V_{FG} = −0.5 V, are compared in Figure 4.13a. For cases (i) and (ii), the electron current in the channel is quite weak, whereas in case (iii) the electron flow between source and drain is clearly amplified (by at least one order of magnitude). Therefore, the critical V_D (~ 0.4 V) can be obtained from the comparison of drain currents between the three types of simulations, as shown in Figure 4.13b.

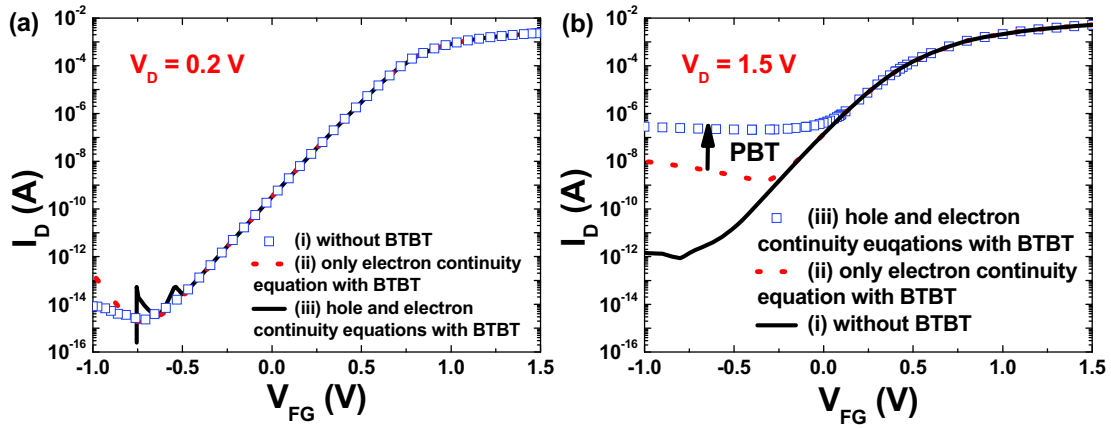

Figure 4.12: *$I_D(V_{FG})$ characteristics for short-channel device simulated with BTBT and hole transport off and on:(a) V_D = 0.2 V and (b) V_D = 1.5 V. T_{si} = 10 nm, W = 2000 nm, L_G = 30 nm and V_{BG} = 0 V.*

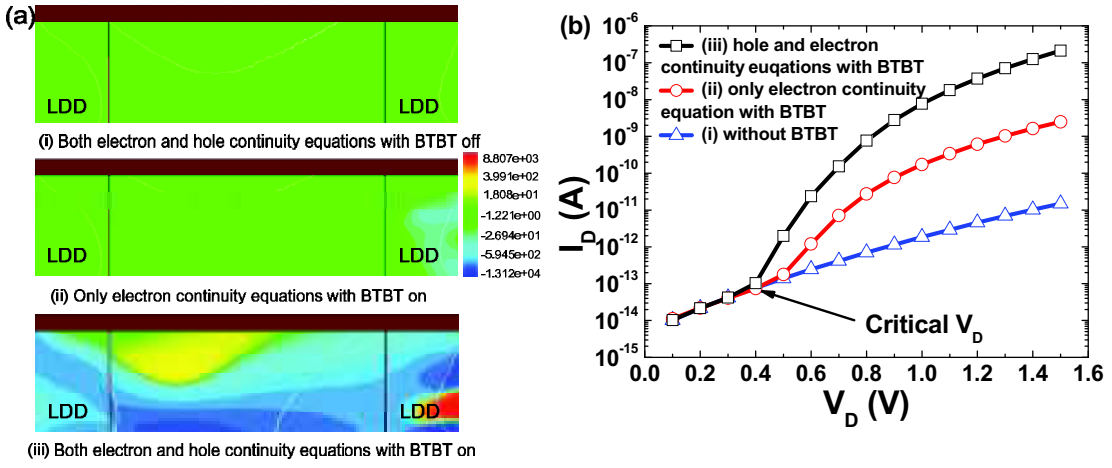

Figure 4.13: *(a) Electron current densities ($A{\cdot}cm^{-2}$) in horizontal direction (from source to drain) for three simulation conditions (V_D = 1.5 V) and (b) $I_D(V_D)$ at V_{FG} = −0.5 V. T_{si} = 10 nm, L_G = 30 nm and V_{BG} = 0 V.*

In order to trigger the parasitic bipolar effect in the ultra-thin FD SOI MOSFETs, there are two bias conditions:

— negative front-gate bias to turn on BTBT generation;
— drain bias larger than critical V_D to reduce the barrier at body-source junction.

Besides the bias, the geometry of device also has an important effect on the parasitic bipolar effect, as demonstrated in the experiments. In next sub-section, we will discuss how the gate length and film thickness affect the parasitic bipolar effect.

2.2.3 Impact of device geometry on current amplification

- **Gate length**

The experiments showed large leakage current only in short-channel devices. Figure 4.14a confirms that no current amplification is visible in long-channel devices. When gate tunneling is neglected, the drain leakage current is clearly dominated by the electron contribution of BTBT current whereas the impact of holes is negligible in long-channel devices. $I_D(V_D)$ curves for long-channel devices are given in Figure 4.14b. No PBT effect happens for any V_D value in long-channel devices; the curves simulated with the hole continuity equation turned on or off tend to superpose. By contrast, in short-channel devices there is a clear increase in drain current when the hole continuity equation is enabled (Figure 4.13b). Therefore, the gate length has an effect on the PBT: the length of MOSFET must be small enough since it plays the role of base. In absence of a short base, the bipolar amplication cannot be possible.

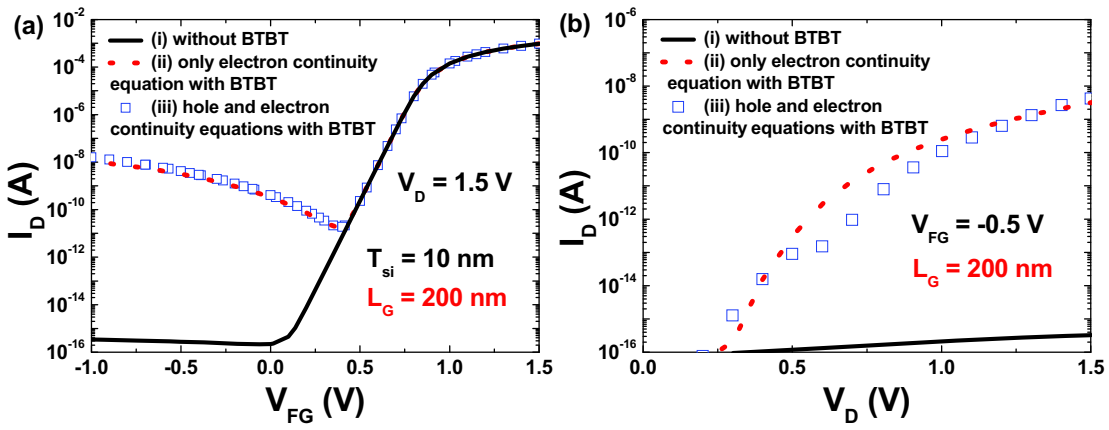

Figure 4.14: *(a) Simulated $I_D(V_{FG})$ and (b) I(V) characteristics in off-state (V_{FG} = −0.5 V) for long-channel devices with V_D = 1.5 V and three scenarios of BTBT.*

Although the parasitic bipolar effect is affected by the gate length, the BTBT generation itself is independent of gate length, which has been experimentally demonstrated in the literature [14], [29], [32]. With BTBT on and only electron continuity equation included, the drain current is equal to the BTBT current. Figure 4.15a compares the drain current between long- and short-channel devices for V_{FG} = −0.5 V. For V_D > 0.4 V, the BTBT current for long-channel device superpose the one for short-channel device. This illustrates that the BTBT generation is indeed independent of gate length. In order to quantify the effect of channel length on BTBT-induced PBT, we define the PBT efficiency η_{PBT} as the ratio of drain currents simulated with hole transport (case (iii)) and without (case (ii)). Above 100 nm gate length, η_{PBT} value saturates to 1, as shown in Figure 4.14b: there is no current amplification due to the transport of holes. In shorter transistors, η_{PBT} increases with $1/L_G$, especially for L_G < 50 nm. For example, in 20 nm long MOSFET the leakage current is amplified by 3 orders of magnitude because of the holes transport.

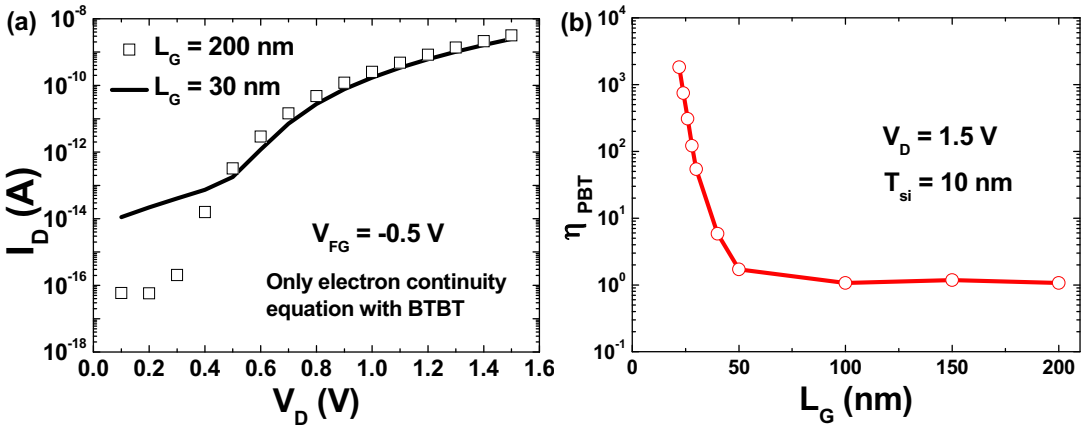

Figure 4.15: *(a) Comparison of drain currents between long- and short-channel devices for V_{FG} = -0.5 V with only electron continuity equation and (b) PBT efficiency η_{PBT} versus gate length L_G.*

- **Film thickness**

The effect of film thickness on PBT is illustrated in Figure 4.16. The simulated characteristics (Figure 4.16a) show the same trend as the experimental curves in Figure 4.8. Decreasing the film thickness effectively helps to suppress the PBT. The extra leakage current induced by PBT almost disappears in 5 nm thick MOSFET (η_{PBT} ≈ 1 in Figure 4.16b). Figure 4.16b suggests that the PBT efficiency increases with thickness, at least in the 5-15 nm range. This can possibly be explained by the more stable body potential in thinner film, leading to the suppression of PBT.

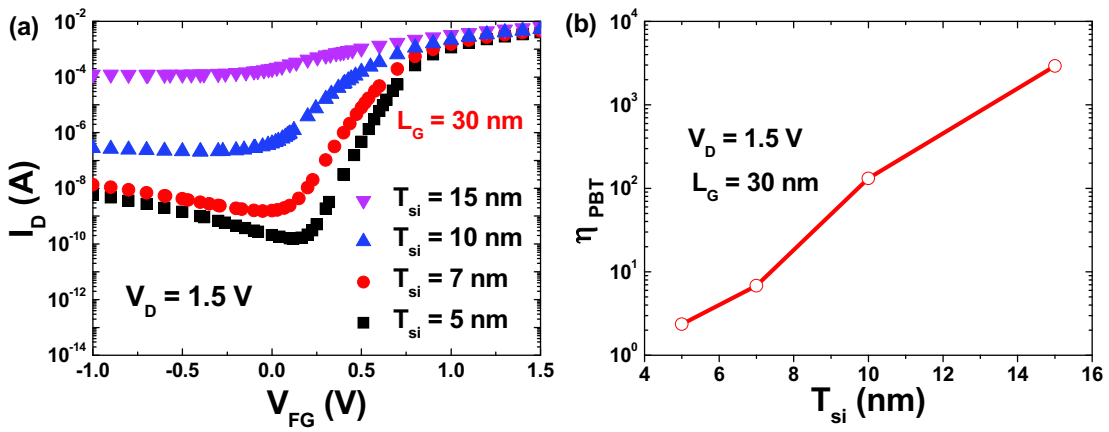

Figure 4.16: *(a) $I_D(V_{FG})$ curves simulated with BTBT and hole transport for different film thickness; (b) PBT efficiency versus film thickness. Synopsys default values for maximum carrier lifetime have been used (τ_n = 10 μs, τ_p = 3 μs).*

In this section, we found the origin of leakage amplification shown in experiments and analyzed how BTBT triggers the parasitic bipolar effect in ultra-thin FD SOI; in next section, we will discuss how to suppress this parasitic bipolar effect.

3. Impact of back-gate on PBT

In order to obtain low OFF-state current, we must suppress this bipolar-enhanced gate-induced drain leakage (GIDL). Many methods to suppress the parasitic bipolar effect have been proposed such as using lower LDD doping concentration to attenuate the electric field in the drain junction [49], Ar ion implantation into source/drain regions to improve the hole diffusion into source [50], Ge-implantation as minority-carrier lifetime killer [51], *etc.* However, all these methods involve additional fabrication steps. In a fabricated FD SOI MOSFET, the BTBT-induced PBT can be suppressed either by reducing the BTBT current (base current) or cutting off the electron path from source to body (or both). In this section, we will show the effect of back-gate on the PBT and how to use it to suppress the PBT.

3.1 Experimental results

In order to evidence the effect of back-gate on the parasitic bipolar effect, we show in Figure 4.17 the characteristics of the sample with thin film (T_{si} = 10 nm). For devices with L_G = 100 nm, the drain leakage does not vary with V_{BG} although the threshold voltage is shifted (Figure 4.17a). A more negative V_{BG} can reduce the drain leakage in short-channel devices (L_G = 30 nm, Figure 4.17b) to the value observed in longer

devices. For even more negative V_{BG} (≤ -3 V), the drain leakage would not improve any longer. This trend indicates that a negative back-gate bias in short devices is effective to attenuate the drain leakage amplified by the lateral PBT until it is fully suppressed.

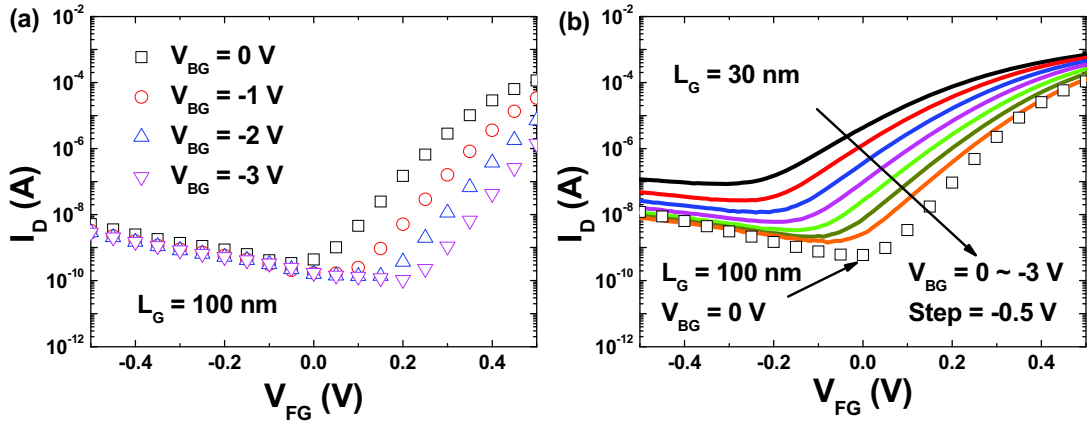

Figure 4.17: *Experimental drain currents for thin samples (T_{si} = 10 nm) versus front-gate voltage with different V_{BG} and V_D = 1.5 V for (a) long-channel and (b) short-channel devices.*

We will discuss in the next sub-section the mechanism of the suppression of the parasitic bipolar effect via the back-gate by using simulations.

3.2 Physical mechanism of suppression of the PBT

Synopsys Sentaurus TCAD simulations aimed to get further insight about the effect of back-gate on the drain leakage. Figure 4.18 shows the simulated drain currents versus front-gate voltage with various V_{BG} for devices with 10 nm film thickness. If BTBT model is deactivated, long and short devices behave similarly and do not show V_{BG} effect on leakage (Figure 4.18a). When BTBT is turned on, the drain leakage for short-channel devices (solid lines in Figure 4.18b) is higher and decreases with negative V_{BG} until it equals to the value for long-channel devices (open symbols in Figure 4.18b). For more negative V_{BG} (≤ -5 V) the drain leakage does not improve any longer. This trend is similar to the experimental results in Figure 4.17b. As already discussed, the existence of BTBT is the starting element for PBT.

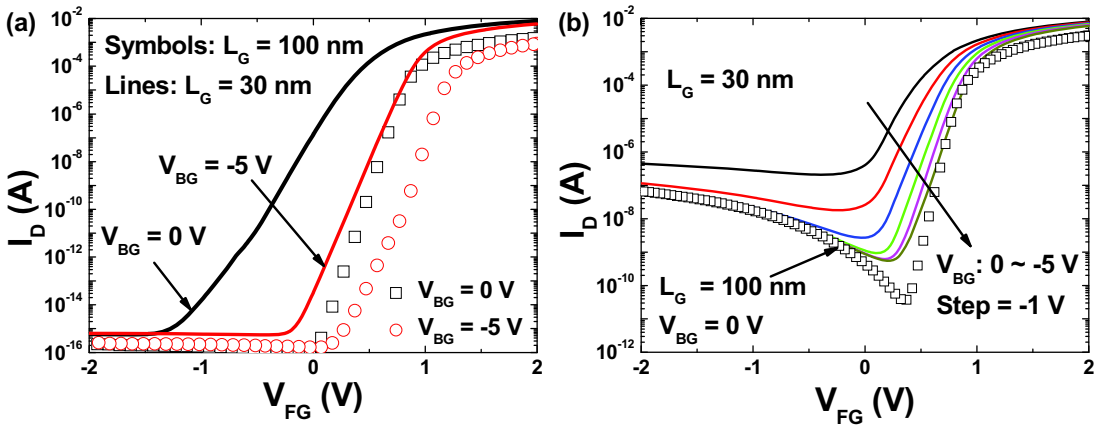

Figure 4.18: *(a) Simulated drain currents without BTBT on for long- and short-channel devices versus front-gate bias under V_{BG} = 0 V and V_{BG} = −5 V. (b) Simulated drain currents with BTBT on for short-channel devices (L_G = 30 nm) versus front-gate voltage with different back-gate bias. T_{si} = 10 nm and V_D = 1.5 V. The open symbols correspond to drain current for long-channel devices (L_G = 100 nm) with V_{BG} = 0 V and V_D = 1.5 V.*

As mentioned in [7], holes generated by BTBT and injected into the body act as the base current, turning on the base-emitter junction; consequently, more electrons from source can flow into the body and be finally collected by the drain. Therefore, in order to cancel the PBT, back-gate must either reduce the BTBT generation or increase the barrier of base-emitter junction (or both). The question is which mechanism is more efficient.

- **BTBT generation**

Figure 4.19 shows the contours of BTBT generation rate with V_{BG} = 0 V and V_{BG} = −5 V for ultra-thin short device (T_{si} = 10 nm, L_G = 30 nm, V_D = 1.5 V and V_{FG} = −1 V). The maximum of BTBT generation rate is of ~ 3.4 × 10^{28} $cm^{-3}\cdot s^{-1}$. A rather similar generation rate is observed in longer channels because BTBT is rather independent on L_G. It is clear that BTBT mainly happens on the top surface of LDD around the drain where the field is stronger; negative back-gate bias has minor effect on the BTBT generation which is governed by the top gate and drain. According to [52], the BTBT current can be calculated from the integration of BTBT generation rate G_{BTBT}:

$$I_{BTBT} = qW \iint G_{BTBT} dxdy \tag{4.4}$$

where G_{BTBT} represents the net generation rate for BTBT and W is the width of the device. Figure 4.20 compares the BTBT currents with V_{BG} = 0 V and V_{BG} = −5 V in

both logarithmic (a) and linear scale (b). Note that the four curves are almost superposed in logarithmic scale (Figure 4.20a). Though BTBT current with V_{BG} = −5 V is a little smaller than the one with V_{BG} = 0 V (Figure 4.20b), the impact of back-gate bias is modest and does not account for the large difference in leakage currents of almost one order of magnitude in Figure 4.18.

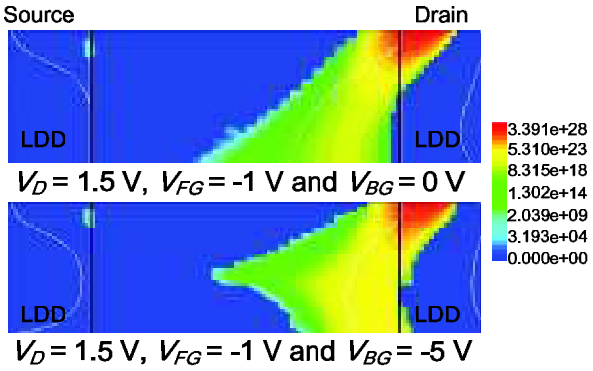

Figure 4.19: *BTBT generation rate contour ($cm^{-3}\cdot s^{-1}$) for V_D = 1.5 V and V_{FG} = −1 V under V_{BG} = 0 V and V_{BG} = −5 V. T_{si} = 10 nm and L_G = 30 nm.*

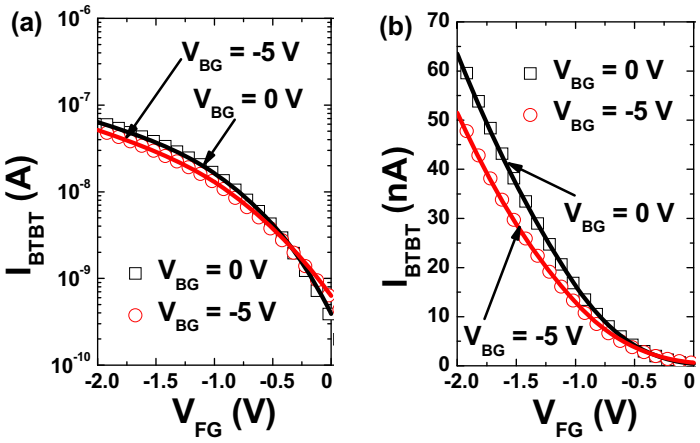

Figure 4.20: *BTBT current versus front-gate voltage for V_D = 1.5 V under different V_{BG} in (a) semi-logarithmic and (b) linear scale. The symbols and solid lines represent the BTBT current for short- and long-devices, respectively. T_{si} = 10 nm and L_G = 30 nm.*

- **Barrier height of body-source junction**

Since it has minor effect on the BTBT generation, the back-gate probably affects the barrier height at body-source junction. In order to verify this aspect, we compare hole density profiles in the channel for two V_{BG} values (V_D = 1.5 V and V_{FG} = −1 V). Although negative V_{BG} makes the holes accumulate at the bottom of the film (Figure 4.21a), the bottom of n-doped LDD tends to be depleted (see the increase of hole

density in the n-doped LDD in Figure 4.21b). This leads to the increase of the barrier height at the source-body junction (E-B), and finally inhibits the PBT activation.

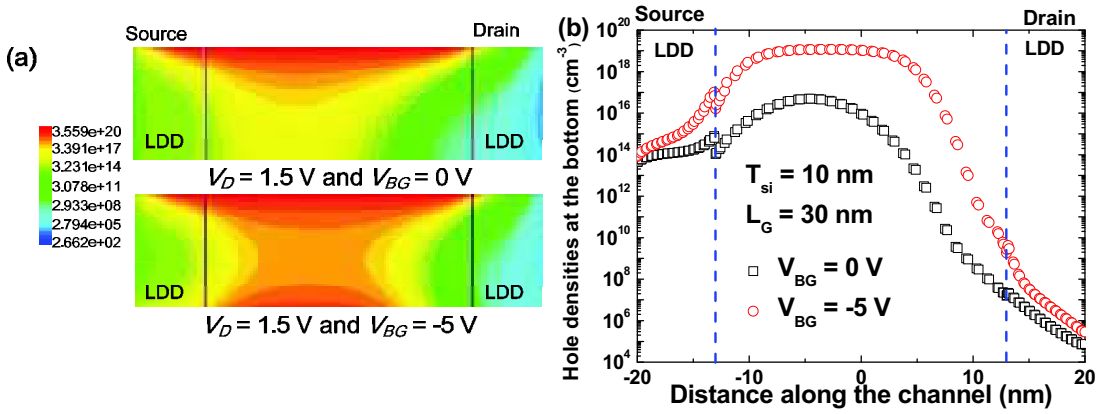

Figure 4.21: *(a) Hole density contours (cm^{-3}) in the whole channel and (b) hole density profile at the bottom interface. V_D = 1.5 V and V_{FG} = −1 V.*

The potential profiles along the channel with V_{BG} = 0 V and V_{BG} = −5 V are compared in Figure 4.22a. An obvious increase of the barrier height at base-emitter junction (body-source junction) is observed when V_{BG} decreases from 0 to −5 V, which helps to prevent electrons leaving the source, as shown in the horizontal electron current densities (Figure 4.22b). Consequently, a negative back-gate bias suppresses the parasitic bipolar effect mainly by increasing the barrier height at body-source junction.

In summary, we evidenced the PBT action in short-channel FD SOI MOSFETs with film thickness down to 7 nm. We proved by simulations, that it is originated from the BTBT-generated holes and it can be suppressed by negative V_{BG}. In the next part of this chapter, we will focus on how to extract the associated bipolar gain.

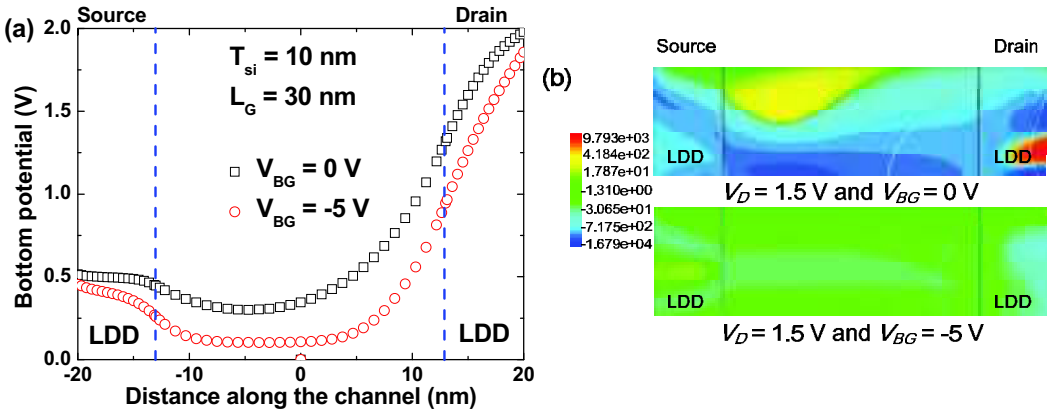

Figure 4.22: *(a) Potential at the Film/BOX interface versus position along the channel and (b) horizontal electron current densities ($A{\cdot}cm^{-2}$) for V_D = 1.5 V and V_{FG} = −1 V.*

4. Extraction of current gain for parasitic bipolar transistor

In a conventional bipolar, one of the important parameters is the common-base current gain β, which reflects the amplification extent of base current. The bipolar gain is defined as the ratio of collector and base currents: $\beta = I_C/I_B$. For a short-channel SOI transistor, the leakage is enhanced by the PBT and therefore the current gain can be used to identify the current contribution from PBT. In addition, the bipolar gain is also a key parameter in the applications of PBT such as I-MOS [53] and Meta-Stable Dip [54].

4.1 Conventional extraction methods

The PBT effect has been characterized by evaluating bipolar gain β in partially-depleted SOI MOFETs, where majority carriers can easily accumulate in the floating body. Several methods to extract β have been developed:

- direct measurement of base current using specific quasi-SOI structures [55];
- high temperature measurements [42];
- pre-breakdown of $I_D(V_D)$ curves [56];
- comparison of drain leakage between short- and long-channel devices [16].

All the four methods proposed earlier for the extraction of the bipolar gain β in relatively thick SOI MOSFETs have been assessed on our ultra-thin FD SOI MOSFETS. The critical problems for the gain extraction are:

- Since no direct access/contact to the body is available to probe the generated hole current (base current), the extraction of bipolar gain based on direct measurement of base current cannot work.
- In modern transistors with very thin dielectric, the gate leakage current masks the BTBT current at moderate V_D (here, $V_D < 1$ V). Therefore, the method based on pre-breakdown of $I_D(V_D)$ curves cannot be applied.
- High temperature easily leads to the breakdown of gate oxide due to large gate leakage, so the method using high temperature measurement fails.

Consequently, only the fourth method, based on the comparison of the drain leakage currents between short- and long-channel transistors, can be adapted. In next sub-

section, we will describe the theoretical background supported by simulations before applying this method to our devices.

4.2 Ratio of drain leakage current between short- and long-channel devices

In long transistors free of the bipolar amplification, the drain leakage current is mainly composed of electron contribution of BTBT generation I_{e_BTBT} and intrinsic MOS current I_{MOS}. In short transistors, the drain current also contains the amplified bipolar contribution I_{e_C} in addition to I_{e_BTBT} and I_{MOS}, as shown in Figure 4.23. Therefore, assuming that the I_{MOS} is small, the bipolar gain can be calculated as:

$$\beta = \frac{I_C}{I_B} = \frac{I_{e\_C}}{I_{h\_BTBT}} = \frac{I_{e\_C}}{I_{e\_BTBT}} = \frac{I_{e\_C} + I_{e\_BTBT}}{I_{e\_BTBT}} - 1 \approx \frac{I_{e\_C} + I_{MOS} + I_{e\_BTBT}}{I_{e\_BTBT} + I_{MOS}} - 1 = \frac{I_{D\_short}}{I_{D\_long}} - 1 \qquad (4.5)$$

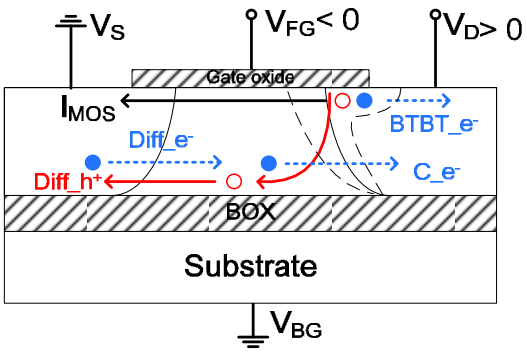

Figure 4.23: *All current flow components in a FD SOI n-channel MOSFET when BTBT-induced PBT occurs. C_e- is the electron diffusion flow reaching the collector. BTBT_e- is the electron flow from BTBT generation. Diff_e- and Diff_h+ are respectively the electron and hole diffusion currents at source-body junction.*

4.2.1 Simulation verification

This appealing method needs validation through simulations. The objective is to physically identify the collector and base currents so that a 'theoretical' bipolar gain can be obtained. The various current contributions are separated using the three types of simulations mentioned above:

(i) without BTBT $\Rightarrow I_{D\_i} = I_{MOS}$;

(ii) BTBT and only electron flow $\Rightarrow I_{D\_ii} = I_{MOS\_e} + I_{e\_BTBT}$;

(iii) BTBT and both hole and electron continuity equations $\Rightarrow$ I_{D_iii} = I_{MOS}+I_{e_BTBT}+I_{e_C}.

These simulations led us to three methods available for calculating the 'theoretical' gain of PBT.

A. Ratio between hole and electron diffusion current at source

According to [57], bipolar gain equals to the ratio between electron and hole diffusion currents of the base-emitter junction:

$$\beta = \frac{I_C}{I_B} = \frac{I_{ediff}}{I_{hdiff}} = \frac{I_{S\_e\_iii} - I_{S\_e\_i}}{I_{S\_h\_iii} - I_{S\_h\_i}} \tag{4.6}$$

Here, I_{S_e,h_iii} are the electron and hole components of source current given by the simulation (iii), whereas I_{S_e,h_i} (equal to $I_{MOS\_e,h}$) are computed from simulation (i). However, this method (method A) only works for simulations, since we cannot separate the electron and hole currents in the experiments.

B. Integration of BTBT generation rate

The base current originates from the hole current generated by BTBT. It can be calculated from the integration of the BTBT generation rate by using Eq. (4.4). The collector current I_C is the difference of drain currents with and without hole continuity equations. Thus, the bipolar gain can be expressed as:

$$\beta = \frac{I_C}{I_B} = \frac{I_{e\_C}}{I_{BTBT}} = \frac{I_{D\_iii} - I_{D\_ii}}{qW\iint G_{BTBT}\,dxdy} \tag{4.7}$$

where I_{D_ii} and I_{D_iii} denote the drain currents obtained from simulations (ii) and (iii). Since the direct measurement of base current (BTBT current) in ultra-thin FD SOI MOSFETs, it is impossible to apply directly this method (method B) to experimental data.

C. Ratio of hole and electron current density in the channel

The base and collector currents flow through the channel, so the integration of horizontal contribution for hole and electron current density in the channel can be

regarded respectively as I_B and I_C. If J_{e,h_iii} and J_{e,h_i} denote the electron and hole current density in the channel direction (in simulation (iii) and (i)), we have:

$$\beta = \frac{I_C}{I_B} = \frac{\iint J_{e\_iii} dxdy - \iint J_{e\_i} dxdy}{\iint J_{h\_iii} dxdy - \iint J_{h\_i} dxdy} \tag{4.8}$$

Since the separation of holes and electrons currents is impossible in experiments, method C cannot be used for experiments. Note that here both I_C and I_B are the horizontal current contribution in the channel, not the total current.

Although methods A, B and C can only be used in simulations, they validate the pragmatic method D based on the ratio of drain current between short- and long-channel devices, as shown in Figure 4.24a. The four methods coincide well in the high injection region (V_D > 0.8 V). The discrepancy in β values for low injection could be explained by the variations of base current for low drain bias. We compare the base current used in the four methods for small drain bias (0.4 V), as shown in Figure 4.24b:

- The base current used in Method A (the hole current of source) is smaller than the one used in Method B (integral BTBT current), which can be attributed to the carriers recombination. Part of holes generated by BTBT recombine in the channel before reaching the source and do not contribute to the base current in Method A, as shown in Figure 4.24c.
- Method B considers the total generated hole current as base current, which leads to a lower β.
- The base current used in Method C (the smallest in Figure 4.24b) is only the horizontal contribution of hole current in the channel, not the total current of the whole device.
- For V_{FG} = −0.5 V and V_D = 0.4 V, the subthreshold current in long-channel device (L_G = 100 nm) is significant and therefore the base current used in Method D (drain current of long-channel device) has the largest value [58], [59].

In high injection (V_D > 1 V), the base current is large enough and the effect of recombination and Short-Channel Effects (SCEs) [58], [59] can be neglected (Figure 4.24d), so all methods yield the same β.

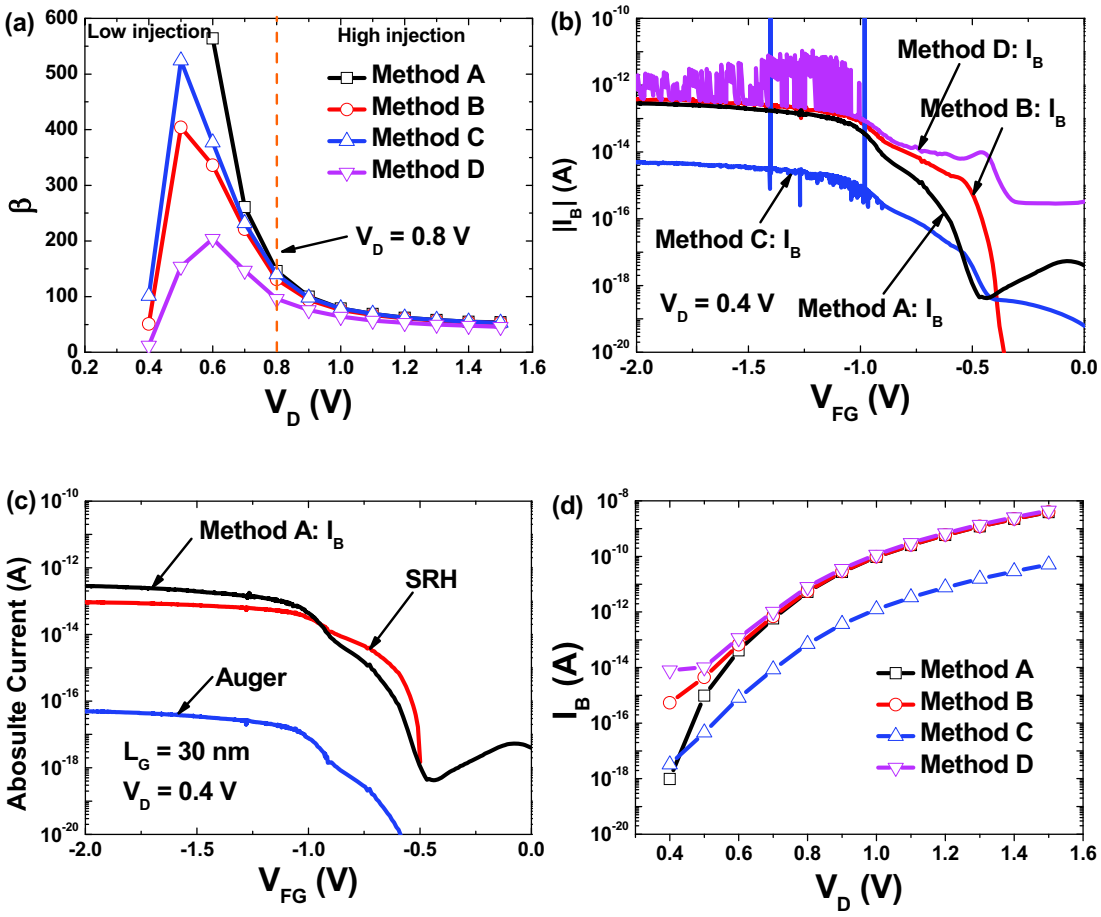

Figure 4.24: *(a) Extracted bipolar gain from simulation results based on the four kinds of methods for V_{FG} = −0.5 V; (b) comparison of base current used in all the four methods for V_D = 0.4 V; (c) comparison of recombination currents and base current used in Method A and (d) comparison of base currents used in the four methods. The practical method D uses the ratio of I_D between long-and short-channel devices (100 nm and 30 nm).*

The key question is what I_D value should be used for the β calculation. In order to minimize the impact of SCEs including subthreshold current and DIBL (see Figure 4.6b) [58], [59], we considered the minimum value instead of I_{D_short} at V_{FG} = −0.5 V for short-channel devices (Figure 4.25a). Since the BTBT is independent of gate length as proved previously, we extract the bipolar gain at a fixed V_{FG}. Therefore, the bipolar gain is extracted as follows:

1) Measure of the minimum value of I_{D_short} for short-channel device (squares in Figure 4.25a).
2) Measure of V_{FG} that yields the minimum value of I_D for short-channel devices (dashed line in Figure 4.25a).
3) Determine the value of I_{D_long} for long-channel device at the same V_{FG} measured

from step (2) (circles in Figure 4.25a).

4) β can be calculated from Eq. (4.5).

The bipolar gains extracted from minimum leakage are given in Figure 4.25b. All curves in Figure 4.25b show that β increases with V_D in low injection and then decreases in high injection [41]. The key message from simulations is that the method to extract β based on the comparison of long- and short-channel devices is validated by the theoretical methods and can be applied to experimental results.

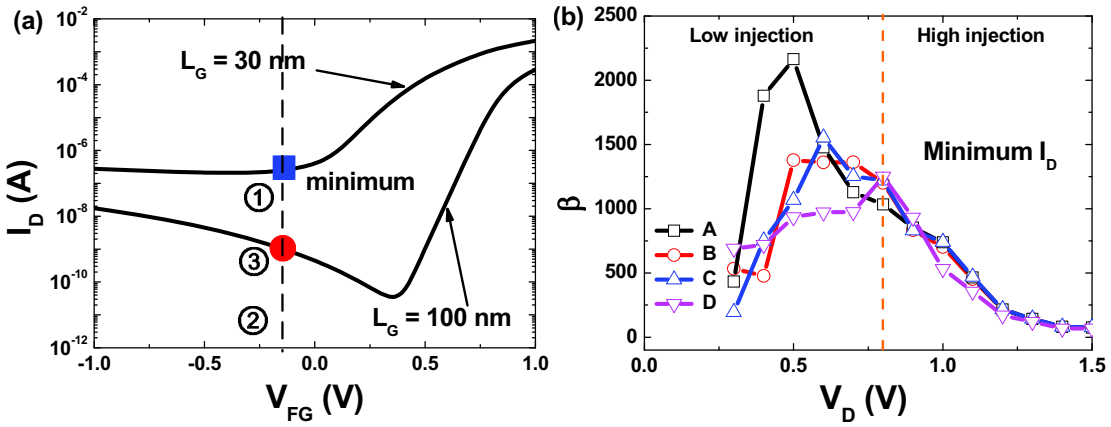

Figure 4.25: *(a) Schematic of simulated $I_D(V_{FG})$ curves for the β extraction based on the ratio of I_D between short- and long-channel devices (V_D = 1.5 V) and (b) extracted bipolar gain from simulation results based on minimum I_D values accounting for the DIBL-induced threshold voltage shift.*

4.2.2 Experimental application

We used 100 nm as 'reference' long-channel MOSFET since for longer devices (L_G = 1000 nm), the drain leakage is masked by the overwhelming gate current (Figure 4.26a). Figure 4.26b shows β derived from the measured curves using Eq. (4.5). In order to minimize the impact of SCEs, we used I_{D_short} values measured at the minimum points of leakage. The extracted β for T_{si} = 10 nm firstly increases and then decreases (V_D > 1.4 V), representing low and high injections respectively. Unfortunately, only a small part of high injection can be observed due to the breakdown of gate oxide for higher V_D. Thinner film (T_{si} = 7 nm) exhibits a smaller bipolar gain, indicating a better electrostatic control.

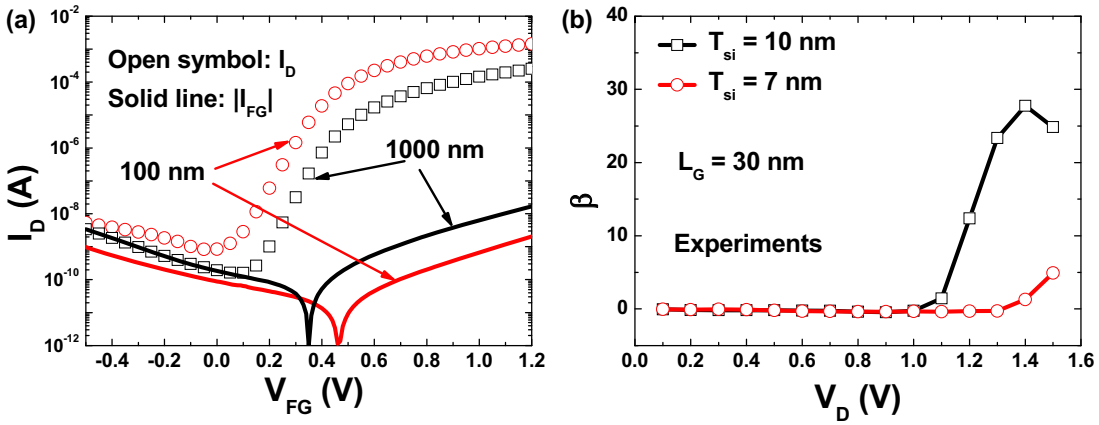

Figure 4.26: *(a) Comparison between drain I_D and gate $|I_{FG}|$ currents measured in long FD SOI MOSFETs (L_G = 1000 nm and 100 nm) at V_D = 1.5 V (T_{si} = 10 nm); (b) experimental bipolar gain β extracted with Eq. (4.5).*

Although the method based on the comparison of OFF-region characteristics of short- and long-channel (free of PBT) devices works in ultra-thin FD SOI MOSFETs, it needs two devices. Note that short-channel MOSFETs suffer from significant variability issues, so does this comparative method. Therefore, an extraction using a single device would be more suitable. In next sub-section, we will propose a new method to extract the bipolar gain based on the effect of back-gate. We proved in section 3 that back-gate can suppress the PBT and next we will use this effect to extract β.

4.3 New extraction method based on back-gate biasing

4.3.1 Extraction principle

Based on the remark that the parasitic bipolar effect is mitigated by a negative V_{BG}, we propose an original method to calculate β. When $V_{BG} \leq -3$ V, the body-source junction is completely turned off, the PBT is fully suppressed, and the main current contribution comes from BTBT current I_{BTBT}. When PBT happens ($V_{BG} > -3$ V), BTBT current acts as base current I_B and the drain current contains the collector current I_C and BTBT current (I_C+I_{BTBT}). Assume that the effect of back-gate on the BTBT current can be neglected, since the generation rate is only lightly modified, as shown in Figure 4.19. Consequently, the bipolar gain β can be calculated as:

$$\beta = \frac{I_C}{I_B} = \frac{I_D - I_{BTBT}}{I_{BTBT}} = \frac{I_D - I_{D\_BG}}{I_{D\_BG}} \tag{4.9}$$

where I_D and I_{D_BG} are respectively the drain leakage currents measured with V_{BG} biased at 0 V and at a value negative enough such that the drain leakage does no longer reduce with V_{BG} because the PBT is fully suppressed.

Before applying this new method (Method E), it is important to discuss the choice of the drain currents used for the calculations in Eq. (4.9). We have noted in Figure 4.17 that with V_{BG} decreasing, the leakage currents in short and long devices tend to merge. However, the minimum I_D values do not coincide, being slightly shifted to the left in short-channel device. This difference can be attributed to the weak inversion current which, in short-channel, is affected by drain-induced barrier lowering and slope degradation [11]. In order to minimize the impact of subthreshold conduction and related SCEs, we do not use the minimum of drain leakage for short-channel devices. Instead, the drain leakage chosen to calculate bipolar gain is the one negatively shifted from the minimum value of drain leakage, as shown in Figure 4.27a. Therefore, the bipolar gain is extracted as follows:

1) Determination of the back-gate voltage for which the leakage current becomes constant with decreasing V_{BG} (V_{BG} = −5V for the simulations in Figure 4.27a).
2) Measure of V_{FG} that yields minimum values of I_D at V_{BG} = 0 V and I_{D_BG} at V_{BG} = −5 V (squares in Figure 4.27a). The difference in V_{FG} accounts for the impact of V_{BG} on threshold voltage and subthreshold slope (interface coupling effect).
3) Negative shift by ΔV_{FG} from the minima of I_D and I_{D_BG} to the values used for extraction, where BTBT is reinforced (circles in Figure 4.27a).
4) β calculation from Eq. (4.9), using the currents corresponding to the V_{FG} identified at step 3 (circles in Figure 4.27a).

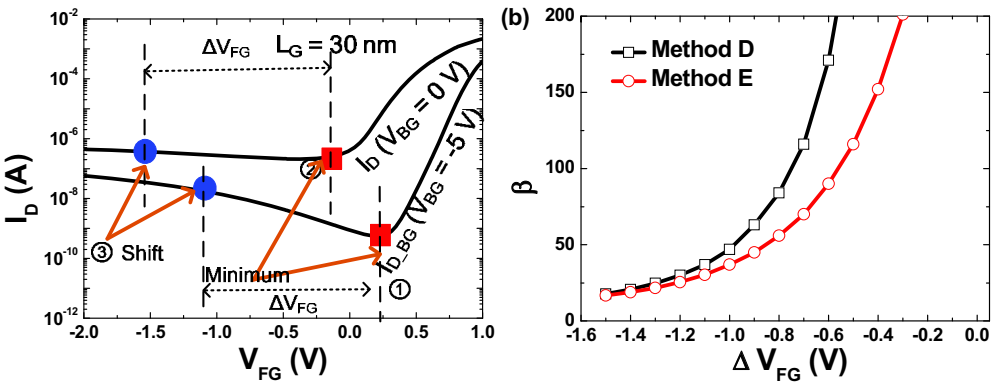

Figure 4.27: *(a) Simulated $I_D(V_{FG})$ curves with the steps for the β extraction and (b) comparison of extracted bipolar gain using methods D and E with various ΔV_{FG}. V_D = 1.5 V.*

For $\Delta V_{FG} \leq -1.2$ V, Method D matches Method E well, as illustrated in Figure 4.27b Figure 4.28a compares the bipolar gain extracted from our new method (Method E) and previous method (Method D) based on the ratio of drain leakage between short- and long-channel devices [16]. I_{D_BG} is the drain leakage simulated with $V_{BG} = -5$ V for Method E. The bell-shaped $\beta(V_D)$ curve is typical for low and strong bipolar injection. It is clear that Method D and Method E exhibit similar variations and actually coincide in the region of interest (high injection, $V_D > 1$ V). According to [7], parasitic bipolar effect is relevant for $V_D > 1$ V when it exceeds other sources of leakage. The difference between the two methods D and E in low injection ($V_D < 1$ V) regime can be attributed to a variation of BTBT generation at negative V_{BG}, which can no longer be neglected as it was for high injection regime.

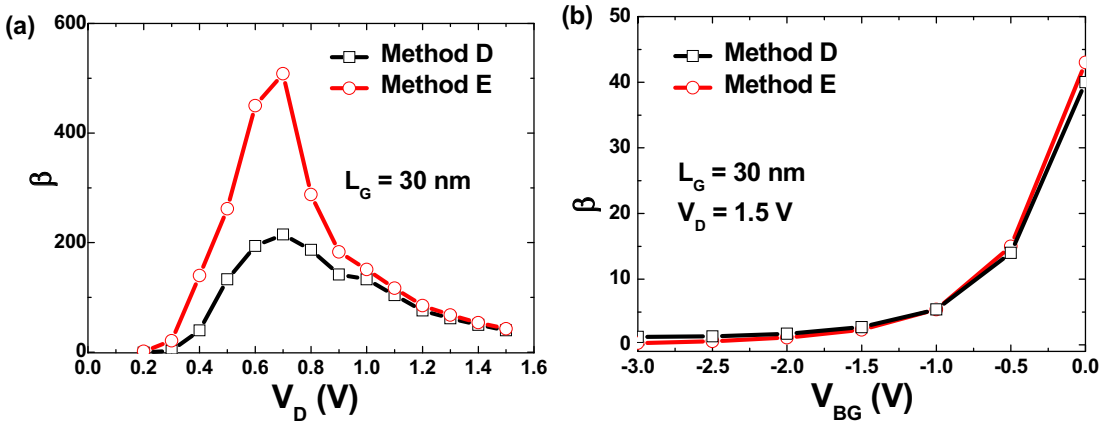

Figure 4.28: *Extracted bipolar gain versus drain bias (a) and back-gate bias (b). Methods D and E show excellent agreement in strong injection. Simulation conditions as in Figure 4.18.* $\Delta V_{FG} = -1.5$ *V.*

Figure 4.29a compares the BTBT generation rate under $V_{BG} = 0$ V and $V_{BG} = -5$ V for a lower drain bias. For $V_{BG} = 0$ V, BTBT mainly happens on the top surface of LDD around the drain; for $V_{BG} = -5$ V, the BTBT generation rate reduces. Therefore, only in strong injection ($V_D > 1$ V), can the effect of back-gate bias on the BTBT generation be neglected (Figure 4.19). This is also reflected in the comparison of drain currents and BTBT currents (Figure 4.29b). I_D for $V_{BG} = 0$ V is always larger than I_{BTBT} under different drain bias. For $V_{BG} = -5$ V, $I_D \approx I_{BTBT}$ only in strong injection ($V_D > 1$ V).

The bipolar gain can be plotted as a function of back-gate bias, as shown in Figure 4.28b. For more negative V_{BG}, the barrier height at body-source junction increases and therefore the bipolar gain decreases to around 1.

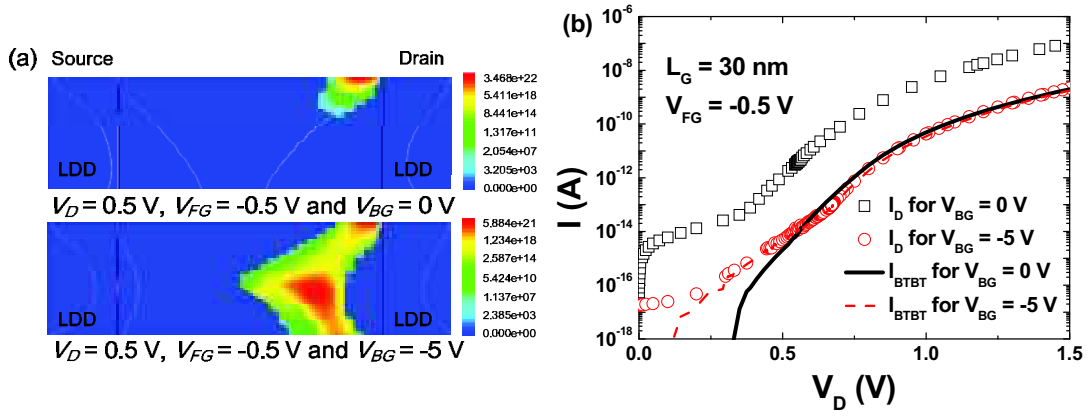

Figure 4.29: *(a) BTBT generation rate contour ($cm^{-3}\cdot s^{-1}$) and (b) comparison of drain currents and BTBT currents for V_D = 0.5 V and V_{FG} = −0.5 V under V_{BG} = 0 V and V_{BG} = −5 V. L_G = 30 nm.*

4.3.2 Experimental application

The devices used in experiments have basically the same structure as in the simulations. The bipolar gain is extracted from the experiments with Eq. (4.9), as shown in Figure 4.30a. Here, I_{D_BG} is the drain leakage for V_{BG} = −3 V. For $\Delta V_{FG} \leq$ −0.15 V, methods D and E coincide well, as illustrated in Figure 4.30b. Measurements at variable V_D are shown in Figure 4.31a. Only the region of low bipolar injection could be observed due to the breakdown of the gate oxide at higher V_D. In order to avoid the impact of gate leakage, we present $I_D(V_{FG})$ measurements performed with V_D = 1.5 V and variable back-gate bias (Figure 4.31b). Nevertheless, the two methods still coincide well in low injection region.

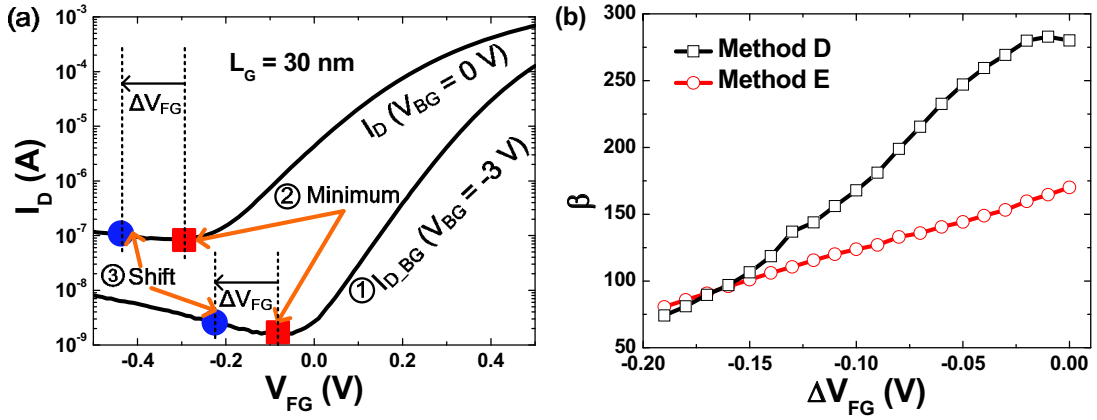

Figure 4.30: *(a) Measured $I_D(V_{FG})$ curves with the steps for the β extraction; (b) comparison of extracted bipolar gain using methods D and E with various ΔV_{FG}. V_D = 1.5 V. ΔV_{FG} = −0.15 V for both methods D and E.*

Figure 4.31 highlights several interesting aspects:

— methods D and E mutually validate each-other;
— the experiment follows the trends anticipated from simulations;
— the bipolar gain is high in sub-30 nm MOSFETs and its contribution to leakage cannot be neglected;
— the bipolar effect can be cancelled with appropriate back-gate bias.

Measurements at variable V_D confirm the transition from weak to strong bipolar injection, as shown in Figure 4.31a.

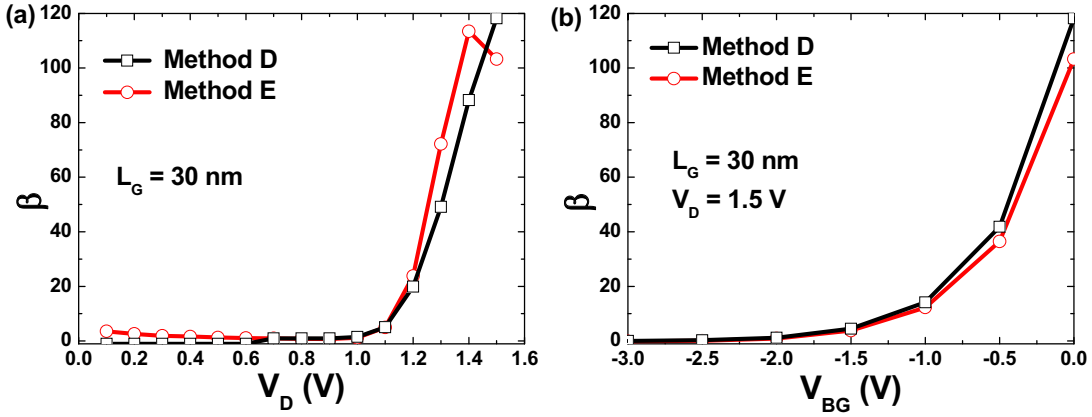

Figure 4.31: *Bipolar gain under different drain bias (a) and back-gate bias (b) extracted from experimental data with Methods D and E. Same device parameters as in Figure 4.17b.*

5. Conclusions and perspectives

The parasitic bipolar effect previously documented in thick film SOI occurs even in ultra-thin MOSFETs. We proved by experiments and simulations that band-to-band tunneling triggers the parasitic bipolar transistor in FD SOI MOSFETs operated in off-state with nominal drain bias. Impact ionization may also cause bipolar action but at higher V_D. The drain leakage amplified by the parasitic bipolar transistor is drastically reduced, even suppressed, in films thinner than 7 nm. For devices with T_{si} = 10 nm, both experiments and simulations show that PBT only happens when L_G < 100 nm. Furthermore V_{BG} biasing was found to reduce PBT.

The comparison of drain leakage currents between long- and short-channel devices is a simple and effective method to extract the gain of the bipolar transistor. This

parameter is important for optimization of device operation and for improving the compact modeling of FD SOI MOSFETs. Our results match the theoretical bipolar gain determined from simulations. In addition, a new method for the extraction of bipolar gain in ultra-thin FD SOI devices has been proposed. This simple method relies on the suppression of the BTBT-induced parasitic bipolar effect under negative back-gate bias. The bipolar gain can be extracted in individual short-channel transistors, without needing a comparison of leakage currents in devices with variable length. Both simulations and experiments confirm this new method.

Future technology nodes aim at obtaining better electrostatic control by thinning down the film to achieve shorter channel length, so the PBT amplification will be a matter of trade-off between these two parameters. Secondly, the ground plane (back-gate bias) is a successful strategy to modulate the threshold voltage in FD SOI MOSFETs. A negative V_{BG} is used in OFF state to increase V_T and lower the static power whereas a positive V_{BG} boosts the ON current by lowering V_T. This strategy is also efficient for adjusting the PBT gain: lower in OFF mode and higher in ON mode. Thirdly, the extracted bipolar gain can be incorporated in compact models for accurate circuit simulation.

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Chapter 5: Coupling effects in three-dimensional SOI devices

The three-dimensional (3D) SOI devices fabricated on SOI substrates exhibits great potential in further down-scaling (sub-20 nm), since they inherit the advantages from both FD SOI and FinFETs [1]–[3]: low subthreshold leakage current, ideal subthreshold swing, high drive current and reduction of short-channel effects. The conventional 3D field effect transistors (FinFETs) has multiple gates [4]. Therefore, in the inversion-mode SOI FinFETs, we must consider the effect of lateral electric field between the two lateral-gates. This lateral electric field which makes the difference between planar and FinFETs enhances coupling effects.

The inversion-mode SOI FinFET is based on the surface inversion of undoped or low-doped channel. With heavily-doped channel, the transistor becomes junctionless (JL) SOI FinFETs [5], [6]. The carrier transport in a JL transistor relies on volume conduction in the partially-depleted body region instead of the conventional surface inversion in MOSFETs. This device is turned off by full depletion of its heavily doped channel. The geometry of channel must be small enough to allow full depletion at a sufficiently low gate voltage. The junctionless transistor can work in three modes: full depletion, partial-depletion and surface accumulation. Thanks to the multiple gates, JL SOI FinFETs will be affected by coupling effect as the inversion-mode SOI FinFETs.

In this chapter, we will take the coupling effect into account in modeling of both inversion-mode and JL SOI FinFETs. In part A, we focus on the modeling of potential and coupling effects in subthreshold region (depletion region for JL transistors). Firstly, we show experimental evidence of coupling effect on inversion-mode vertical double-gate (DG) SOI FinFETs. Based on the two-dimensional (2D) potential distribution in subthreshold region, an analytical model of threshold voltage will be developed by considering the coupling effects. Secondly, we will adapt this 2D potential model to JL SOI FinFETs.

In part B, we propose a compact model of carrier profile for single-, double- and triple-gate JL transistors in partial depletion region. Using this very simple model, we determine threshold voltage and maximum body size enabling full depletion. In addition, we develop two methods to extract the flat-band voltage, low-field mobility and doping concentrations in “weak” accumulation region. In part C, we apply the proposed methods to the experimental data of GaN junctionless FinFETs.

Part A: Modeling of potentials and coupling effects in inversion-mode and junctionless SOI FinFETs

1. Coupling effects in inversion-mode vertical DG SOI FinFETs

In planar FD SOI MOSFETs, front- or back-channel threshold voltage can be changed by the opposite gate biasing which can be used for dynamic threshold voltage control. This phenomenon is well known as coupling effect between front- and back-gates [7], [8]. Moreover, in inversion-mode SOI FinFETs, especially in narrower fin, the lateral-gates will affect the potential in the body, modifying the coupling effects between top- and back-gates. Understanding these coupling effects and modeling them accurately is of great importance for applications. For example, increasing threshold voltage can reduce leakage current and power consumption. Conversely, lower operating bias is achieved with reduced threshold voltage. Also, we can co-integrate different functions in the same chip by tuning the threshold voltage. In this section, we will experimentally show coupling effect in vertical DG SOI FinFETs and develop an analytical model for it.

1.1 Experiments

1.1.1 Device fabrication

The inversion-mode SOI FinFETs have vertical double-gate (DG) structure (Figure 5.1), fabricated at SEMATEC. SiO_2 (1 nm) and HfO_2 (2.5 nm) layers were stacked for lateral-gate insulators (EOT = 1.4 nm). At the top of the fin, SiO_2 (5 nm) and thick nitride (10 nm) layers were deposited to prevent the top-channel conduction. The two lateral-gates are controlled by the same bias. The film thickness is of 40 nm and the BOX is of 140 nm. We selected the long-channel (L_G = 500 nm) devices to remove the SCEs and focus on coupling effects. The fin width varies from 25 nm to 500 nm. All the devices have undoped body and TiN metal gate.

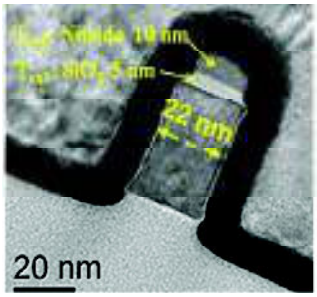

***Figure 5.1*:** *TEM cross section of the vertical DG FinFET fabricated on the SOI wafer.*

1.1.2 Experimental evidence of coupling effect

The 'vertical' coupling effect between the two lateral-channels and the back-gate bias was systematically investigated in our fully-depleted vertical DG FinFETs. These devices can be operated with one, two and/or three channels by applying appropriate bias at front- and/or back-gates. Since the top dielectric stack is thick, the top-channel is inhibited and does not have any impact on the transport if front-gate stays low enough. The coupling effect will lead to the variations of front and back threshold voltages.

- **Front-channel coupling effect**

In Figure 5.2, we compare the front-channel transconductance curves at different back-gate bias (from −15 V to +15 V) in wide (W_{fin} = 500 nm) and narrow (W_{fin} = 80 nm) fins. For wide fin device (W_{fin} = 500 nm, Figure 5.2a), when the back-gate interface moves from accumulation to inversion regime (from −15 V to +15 V), a large shift of the transconductance curve towards lower front-gate voltage is observed. At positive back-gate bias (> +3 V), a hump appears in the transconductance curve reflecting the early activation of the back-channel. As the fin width becomes sufficiently small (Figure 5.2b), the influence of the two lateral-gates prevails, attenuating the back-gate effect (smaller lateral shift of $g_m(V_{FG})$ curves with V_{BG}). The activation of the back-channel is barely visible for V_{BG} = +15 V.

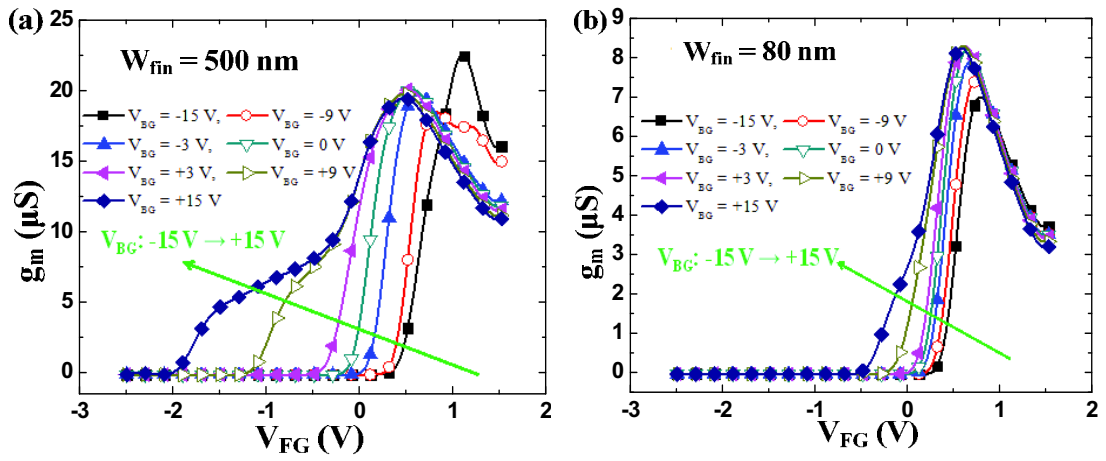

Figure 5.2: *Front-channel coupling effects in vertical DG FinFET. Transconductance as a function of the front-gate bias at different back-gate bias in (a) wide (W_{fin} = 500 nm) and (b) narrow (W_{fin} = 80 nm) fin devices. L_G = 500 nm, N_F = 2, V_D = 0.05V. N_F denotes the number of fins.*

- **Back-channel coupling effect**

Figure 5.3 highlights the reciprocal effect of the front-gate bias on the back-channel transconductance in wide (W_{fin} = 500 nm) and narrow (W_{fin} = 80 nm) fin devices. As it was already observed with the front-channel transconductance, when the front-gate bias changes from accumulation to inversion V_{FG} (from −1 V to +1 V), a large shift of the transconductance curve towards lower back-gate voltage is observed in a wide fin (Figure 5.3a). Unlike the front-channel transconductance characteristics shown in Figure 5.2, the lateral shift is more pronounced in narrow fins where the sidewall gates dominate (Figure 5.3b).

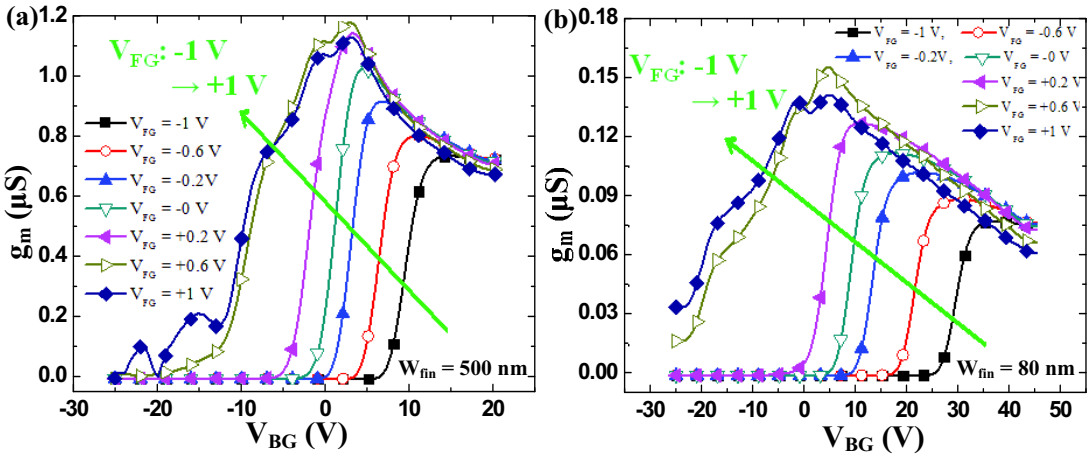

Figure 5.3: *Back-channel coupling effects in vertical DG FinFETs. Transconductance versus back-gate bias at different front-gate bias in (a) wide (W_{fin} = 500 nm) and (b) narrow (W_{fin} = 80 nm) fin devices. L_G = 500 nm, N_F = 2, V_D = 0.05V.*

One peak only, corresponding to the back-channel activation, is observed on the trasnconductance curve in both wide and narrow fin for $V_{FG} \leq 0$ V (when the lateral-channels are depleted or accumulated). However, at positive front-gate bias ($V_{FG} \geq$ +0.6 V), the transconductance curves show multiple features which suggest that the lateral channel is not homogeneous along the fin height. The upper region is activated before the lower region of the sidewalls which are in contact with the accumulated back-interface. The hump (at $V_{BG} \approx -15$ V) reflects the conduction in the lateral-channel regions located far from the back-interface. The next peak (at $V_{BG} \approx -3$ V) indicates the completion of the lateral-channels. The third peak ($V_{BG} > 0$ V) is generated by the activation of the back-channel.

- **Effect of coupling effect on threshold voltage**

The coupling effects shown previously strongly affect the threshold voltage. Figure 5.4 shows the threshold voltage for various fin widths in different electrostatic configurations. The threshold voltages were extracted with the Y-function method [9] and plotted versus the opposite gate bias and fin width. It is clear that, in wide fin devices, the coupling effect between back- and top-gates (V_{THF} versus V_{BG}) is enhanced. In narrow fin devices, the lateral electric field induced by the two side gates is able to control the potential at the body/BOX interface. Therefore, the 'vertical' field from bottom to top, generated by the back-gate bias, is blocked by the enhanced 'lateral' field. Consequently, the capability of the back-gate to modulate the front-channel properties is declining in narrower fins. This is why the lateral shift and hump of the transconductance curves are reduced (Figure 5.2a and b) and the impact of back-gate is smaller (Figure 5.4a) in the narrow device.

The effect of front-gate on the back threshold voltage is different from that of back-gate on the front threshold voltage. In a narrower fin, the back-channel threshold voltage increases more significantly for negative front-gate bias (Figure 5.4b). This can be attributed to the accumulation layer near the body/BOX interface when the front-gate bias is more negative. This makes it more difficult for the back-gate to invert the back interface, hence the back threshold voltage increases remarkably.

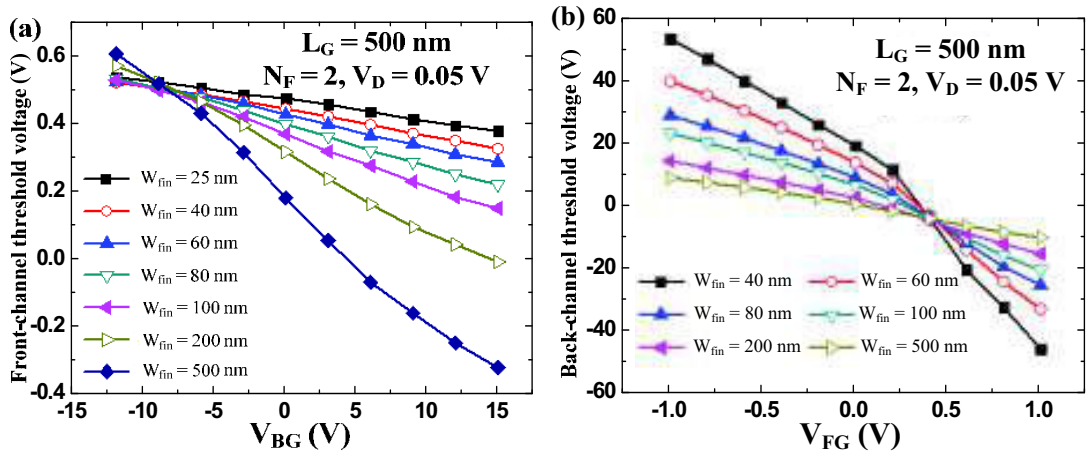

Figure 5.4: *Coupling effects dependence on the fin width. (a) Front- and (b) back-channel threshold voltage as a function of the opposite gate bias for different fin widths.*

We have experimentally evidenced the coupling effects in vertical DG FinFETs and found that the coupling effects between front- and back-gates decrease with fin width

shrinking. In next sub-section, we will develop a 2D analytical model in order to predict the effect of coupling effect on threshold voltage.

1.2 Analytical model

The analytical model for the coupling effect between front- and back-gates was firstly proposed by Lim and Fossum [7]. However, this one-dimensional model only works in planar FD SOI MOSFETs. In 2007, Akarvardar *et al.* extended this model to a 2D coupling model in inversion-mode triple-gate SOI FinFETs [10]. In this sub-section, we will adapt the 2D coupling model to the inversion-mode vertical DG SOI FinFETs. Based on our analytical model, the effect of coupling effect on front and back threshold voltage can be evaluated and anticipated.

1.2.1 Potential distribution

In the 2D analytical model of triple-gate SOI FinFETs proposed by Akarvardar *et al.* [10], a parabolic potential variation between the two lateral-gates is assumed. However, in our vertical DG FinFETs, the thickness of top-gate oxide (T_{tox}) is different from the one of lateral-gates oxide (T_{lox}), as shown in Figure 5.5. The two lateral-gates are connected together and have the same thickness of gate oxide. Therefore, we still assume that the potential profile between the two lateral-gates is parabolic in the vertical DG FinFETs:

$$\varphi(x,y) = a(y)x^2 + b(y)x + c(y) \tag{5.1}$$

where $\varphi(x,y)$ is the 2-D body potential in undoped body.

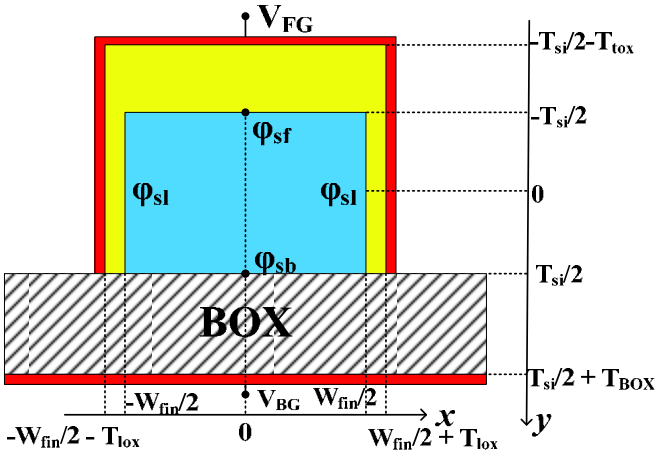

Figure 5.5: *Cross-section of a vertical DG SOI FinFET, showing the symbols and axes used for modeling.*

The coefficients of Eq. (5.1) are determined using the boundary conditions at the lateral-gates:

$$\varphi(-W_{fin}/2, y) = V_{FG} - V_{FBF} + \frac{\varepsilon_{si}}{C_{lox}} \frac{\partial \varphi(x, y)}{\partial x}\bigg|_{x=-W_{fin}/2} \tag{5.2}$$

$$\varphi(W_{fin}/2, y) = V_{FG} - V_{FBF} - \frac{\varepsilon_{si}}{C_{lox}} \frac{\partial \varphi(x, y)}{\partial x}\bigg|_{x=W_{fin}/2} \tag{5.3}$$

Here, V_{FBF} is flat band voltage for front-gate, ε_{si} is the silicon permittivity, C_{lox} is the capacitance per unit area for the oxide of lateral-gates and W_{fin} is the width of the fin. Since the two lateral-gates are identical, so are the surface potentials: $\varphi(-W_{fin}/2, y) = \varphi(W_{fin}/2, y) = \varphi_{sl}$. Assume that corner effects, quantum-mechanical effects, substrate depletion (under the BOX) and drain bias effect can be ignored [10], [11]. Using Eqs. (5.1)-(5.3), we obtain the coefficients in Eq. (5.1) as:

$$\begin{aligned} a(y) &= \frac{V_{FG} - V_{FBF} - \varphi(0, y)}{\frac{W_{fin}^2}{4} + \frac{\varepsilon_{si}}{C_{lox}} \cdot W_{fin}} = \frac{V_{FG} - V_{FBF} - \varphi(0, y)}{2W_0^2} \\ b(y) &= 0 \\ c(y) &= \varphi(0, y) = \varphi_{sf} \end{aligned} \tag{5.4}$$

In order to simplify the calculation, we define $\eta_0 = \varepsilon_{si}/C_{lox}W_{fin}$ and $W_0 = \sqrt{1/8 + \eta_0/2} \cdot W_{fin}$. η_0 is actually equal to the ratio between C_{fin} and C_{lox}. $C_{fin} = \varepsilon_{si}/W_{fin}$ is the "lateral" channel capacitance per unit area defined in the 2D model of triple-gate SOI FinFETs [10]. Therefore, Eq. (5.1) can be rewritten as:

$$\varphi(x, y) = \left(1 - \frac{x^2}{2W_0^2}\right)\varphi(0, y) + \frac{V_{FG} - V_{FBF}}{2W_0^2} x^2 \tag{5.5}$$

Since the channel is undoped in our vertical DG FinFETs, the body doping can be safely neglected in the subthreshold region and the electrostatic potential in the depletion region satisfies the 2D Laplace equation:

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} + \frac{\partial^2 \varphi(x, y)}{\partial y^2} = 0 \tag{5.6}$$

Substituting Eq. (5.5) into Eq. (5.6) and letting $x = 0$, we have:

$$-\frac{1}{W_0^2}\varphi(0, y) + \frac{V_{FG} - V_{FBF}}{W_0^2} + \frac{d^2 \varphi(0, y)}{dy^2} = 0 \tag{5.7}$$

The solution of Eq. (5.7) has the form of:

$$\varphi(0,y)=C_1\,sinh\left(\frac{y}{W_0}\right)+C_2\,cosh\left(\frac{y}{W_0}\right)+V_{FG}-V_{FBF} \tag{5.8}$$

Here, C_1 and C_2 are the coefficients determined by the boundary conditions of the top and bottom interface, which can be described as:

$$\varphi(0,-T_{si}/2)=V_{FG}-V_{FBF}+\frac{\varepsilon_{si}}{C_{tox}}\frac{\partial\varphi(0,y)}{\partial y}\Big|_{y=-T_{si}/2} \tag{5.9}$$

$$\varphi(0,T_{si}/2)=V_{BG}-V_{FBB}-\frac{\varepsilon_{si}}{C_{BOX}}\frac{\partial\varphi(0,y)}{\partial y}\Big|_{y=T_{si}/2} \tag{5.10}$$

in which V_{FBB} is the flat-band voltage for back-channel, C_{BOX} and C_{tox} are respectively the capacitance per unit area for BOX and the thick oxide of top-gate. After inserting the boundary conditions, we can obtain the coefficients in Eq. (5.8) as:

$$\begin{aligned}
C_1&=\frac{\left(V_{BG}-V_{FBB}-V_{FG}+V_{FBF}\right)\cdot\left[\cosh\left(\frac{T_{si}}{2W_0}\right)+\frac{\varepsilon_{si}}{C_{tox}W_0}\cdot\sinh\left(\frac{T_{si}}{2W_0}\right)\right]}{\left(1+\frac{\varepsilon_{si}}{C_{tox}W_0}\cdot\frac{\varepsilon_{si}}{C_{BOX}W_0}\right)\cdot\sinh\left(\frac{T_{si}}{W_0}\right)+\left(\frac{\varepsilon_{si}}{C_{tox}W_0}+\frac{\varepsilon_{si}}{C_{BOX}W_0}\right)\cdot\cosh\left(\frac{T_{si}}{W_0}\right)}\\
C_2&=\frac{\left(V_{BG}-V_{FBB}-V_{FG}+V_{FBF}\right)\cdot\left[\sinh\left(\frac{T_{si}}{2W_0}\right)+\frac{\varepsilon_{si}}{C_{tox}W_0}\cdot\cosh\left(\frac{T_{si}}{2W_0}\right)\right]}{\left(1+\frac{\varepsilon_{si}}{C_{tox}W_0}\cdot\frac{\varepsilon_{si}}{C_{BOX}W_0}\right)\cdot\sinh\left(\frac{T_{si}}{W_0}\right)+\left(\frac{\varepsilon_{si}}{C_{tox}W_0}+\frac{\varepsilon_{si}}{C_{BOX}W_0}\right)\cdot\cosh\left(\frac{T_{si}}{W_0}\right)}
\end{aligned} \tag{5.11}$$

In order to simplify the solution of Eq. (5.7), we define $\eta_1=\varepsilon_{si}/(C_{tox}W_0)$ and $\eta_2=\varepsilon_{si}/(C_{BOX}W_0)$. Substituting Eq. (5.11), η_1 and η_2 into Eq. (5.8), we have:

$$\begin{aligned}
&\varphi(0,y)=\left(V_{BG}-V_{FBB}-V_{FG}+V_{FBF}\right)F(y)+V_{FG}-V_{FBF}\\
&\text{with } F(y)=\frac{\sinh\left[\left(y+T_{si}/2\right)/W_0\right]+\eta_1\cosh\left[\left(y+T_{si}/2\right)/W_0\right]}{\left(1+\eta_1\eta_2\right)\sinh\left(T_{si}/W_0\right)+\left(\eta_1+\eta_2\right)\cosh\left(T_{si}/W_0\right)}
\end{aligned} \tag{5.12}$$

Substituting Eq. (5.12) into Eq. (5.5) yields the 2D potential distribution as:

$$\varphi(x,y)=\left(V_{BG}-V_{FBB}-V_{FG}+V_{FBF}\right)\left(1-\frac{x^2}{2W_0^2}\right)F(y)+V_{FG}-V_{FBF} \tag{5.13}$$

1.2.2 Validation by simulations

In order to validate our 2D potential model, Synopsys Sentaurus TCAD is employed for simulations [12]. The simulated structure is the same as in Figure 5.5. Here, we used 30 nm and 1.4 nm thick SiO_2 layers for the top- and lateral-gate insulator. Fin height is 40 nm and the thickness of BOX is 140 nm. The doping concentration of channel is of 10^{15} cm^{-3} and the doping concentration of source/drain is of 10^{20} cm^{-3}. The back-gate contact is directly placed on bottom of BOX in order to avoid the any effect of substrate. The gate length is fixed as 500 nm to eliminate short-channel effects. The width of channel varies from 40 nm to 80 nm.

The Philips Unified Mobility Model used in the simulations describes the mobility degradation due to the impurity scattering mechanism. The velocity saturation is considered in high-field mobility model (*Canali* model by default). *Enormal* mobility model used includes the surface scattering. The Shockley-Read-Hall recombination and Auger recombination are also included. The work-functions of the front- and back-gate are set to make the flat-band voltages (V_{FBF} and V_{FBB}) equal to zero. For accurate results, the advanced hydrodynamic simulation is used. The drain is biased at 0.05 V.

TCAD simulations demonstrate that the shape of potential along *x* direction is indeed parabolic in an n-channel vertical DG FinFET, as shown in Figure 5.6a. Figure 5.6b shows the 2D body potential profiles calculated from the model. It reproduces the simulated potential distribution in the channel (Figure 5.6a). Figure 5.7 compares 1D potential profiles in the fin for different front/back-gate voltages. An excellent agreement can be seen between the modeled and simulated results.

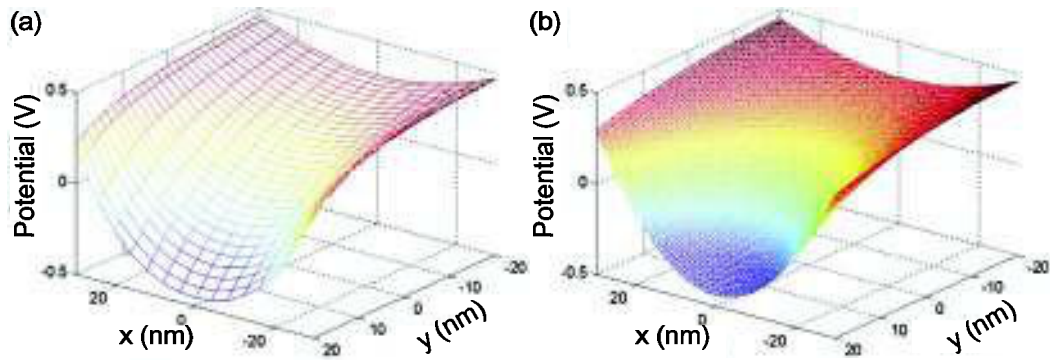

Figure 5.6: *2D body potential distributions in DG FinFETs: (a) simulation and (b) model. T_{tox} = 30 nm, T_{lox} = 1.4 nm, T_{si} = 40 nm, T_{BOX} = 140 nm, L_G = 500 nm and W_{fin} = 50 nm. V_D = 0.05 V.*

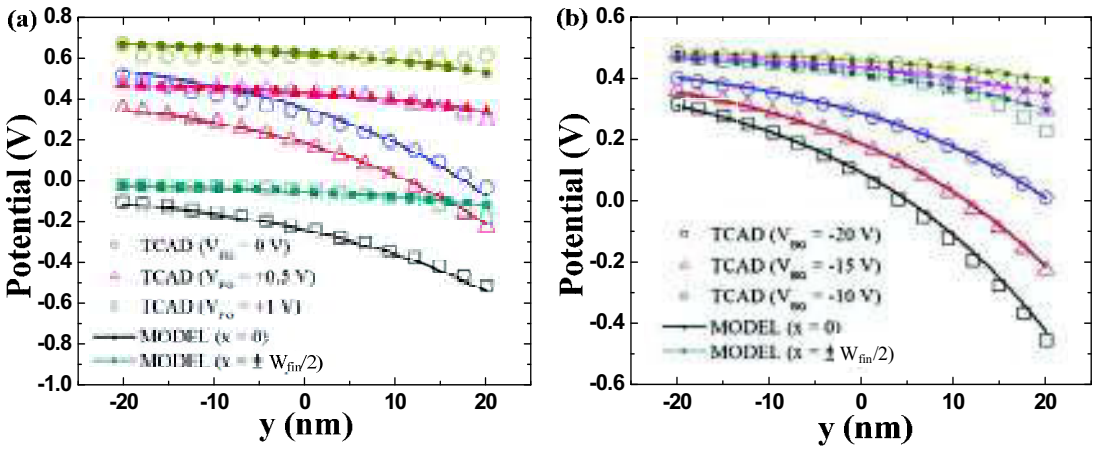

Figure 5.7: *Potential profiles along $x = 0$ and $x = \pm W_{fin}/2$ as functions of (a) the front-gate voltage and (b) the back-gate voltage. $V_D = 0.05$ V.*

1.2.3 Application of 2D analytical model

The 2D body potential distribution is useful to quantify the threshold voltages of front-/back-channel (V_{THF}/V_{THB}). Firstly we discuss the front-channel threshold voltage. In vertical DG FinFETs, the front-gate voltage is linked to the maximum of surface potential at front-gate (φ_m) [11]. From Eq. (5.13), we determine φ_m at $(x, y) = (-W_{fin}/2, -T_{si}/2)$ or $(x, y) = (W_{fin}/2, -T_{si}/2)$, as shown in Figure 5.6. Here, we use:

$$\varphi\left(W_{fin}/2,\ -T_{si}/2\right)=\varphi_m \tag{5.14}$$

Substituting Eq. (5.14) into Eq. (5.13) yields:

$$\begin{aligned}&\varphi_m=\left(V_{BG}-V_{FBB}-V_{FG}+V_{FBF}\right)\cdot\lambda\cdot F(-T_{si}/2)+V_{FG}-V_{FBF}\\&\text{with }\lambda=\frac{4}{4+1/\eta_0}=\frac{4}{4+C_{lox}/C_{fin}}\end{aligned} \tag{5.15}$$

where $C_{fin} = \varepsilon_{si}/W_{fin}$ is the "lateral" capacitance per unit area, reflecting the 2D aspect of our model [10]. When the front-gate governs the channel, the minimum of surface potential for back-gate always appears at $(x, y) = (0, T_{si}/2)$, as shown in Figure 5.6:

$$\varphi_{sb}=\varphi\left(0,\ T_{si}/2\right)=\left(V_{BG}-V_{FBB}-V_{FG}+V_{FBF}\right)F(T_{si}/2)+V_{FG}-V_{FBF} \tag{5.16}$$

Combining Eqs. (5.15) and (5.16), we can express the front-gate voltage as:

$$V_{FG}=\varphi_m+V_{FBF}+\frac{\lambda F(-T_{si}/2)}{F(T_{si}/2)-\lambda F(-T_{si}/2)}\cdot\left(\varphi_m-\varphi_{sb}\right) \tag{5.17}$$

The back-gate voltage can be obtained by substituting Eq. (5.17) into Eq. (5.16):

$$V_{BG} = \varphi_{sb} + V_{FBB} - \frac{1 - F(T_{si}/2)}{F(T_{si}/2) - \lambda F(-T_{si}/2)} \cdot \left(\varphi_m - \varphi_{sb}\right) \tag{5.18}$$

- **Threshold voltage for front-gate**

The threshold voltage for front-gate is determined by replacing V_{FG} with V_{THF} and letting $\varphi_m = \varphi_{inv}$ in Eq. (5.17).

$$V_{THF} = \varphi_{inv} + V_{FBF} + \frac{\lambda F(-T_{si}/2)}{F(T_{si}/2) - \lambda F(-T_{si}/2)} \cdot \left(\varphi_{inv} - \varphi_{sb}\right) \tag{5.19}$$

where φ_{inv} denotes the potentials at the strongly inverted silicon surfaces. According to [10], $\varphi_{inv} = \varphi_F + \varphi_T$ for $N_A \geq 2 \times 10^{17}$ cm^{-3} and $\varphi_{inv} = 2\varphi_F$ for $N_A < 2 \times 10^{17}$ cm^{-3}. φ_T denotes the band bending with respect to Fermi level at $(x, y) = (-W_{fin}/2, -T_{si}/2)$ [13]–[15]. Since the measured vertical DG FinFET is undoped, we assume a single front or back interface value at threshold voltage ($\varphi_{inv} = 2\varphi_F$). Depending on the charge state at the back interface, the expression of threshold voltage for front-gate is divided into three generic cases.

1) For an accumulated back interface, $\varphi_{sb} = 0$, leading to

$$V_{THF} = V_{FBF} + \frac{F(T_{si}/2)}{F(T_{si}/2) - \lambda F(-T_{si}/2)} \cdot 2\varphi_F \tag{5.20}$$

2) For an inverted back interface, $\varphi_{sb} = 2\varphi_F$, yielding

$$V_{THF} = V_{FBF} + 2\varphi_F \tag{5.21}$$

3) For a depleted back interface, φ_{sb} depends on V_{BG} and is solved from Eq. (5.18) by imposing $\varphi_m = 2\varphi_F$. Substituting the calculated φ_{sb} into Eq. (5.19), we have:

$$V_{THF} = V_{FBF} - \xi \cdot \left(V_{BG} - V_{FBB}\right) + \left(1 + \xi\right) \cdot 2\varphi_F \tag{5.22}$$

where

$$\xi = \frac{\alpha F(-T_{si}/2)}{1 - \alpha F(-T_{si}/2)} = \left|\frac{dV_{THF}}{dV_{BG}}\right| \tag{5.23}$$

is the "front coupling effect coefficient" defined as the slope (in absolute value) of $V_{THF}(V_{BG})$ characteristic for a depleted back interface [7], [10].

- **Threshold voltage for back-gate**

Similarly, the expression of the back-gate threshold voltage can be derived from reciprocal of Eqs. (5.17) and (5.18) when the front-gate is biased in inversion, depletion and accumulation states, shown as follows:

$$V_{THB} = \begin{cases} V_{FBB} + \dfrac{1-\lambda F(-T_{si}/2)}{F(T_{si}/2)-\lambda F(-T_{si}/2)} \cdot 2\varphi_F, & \text{Accmulated front interface} \\ V_{FBB} + 2\varphi_F, & \text{Inverted front interface} \\ V_{FBB} - \zeta\left(V_{FG} - V_{FBF}\right) + \left(1+\zeta\right) \cdot 2\varphi_F, & \text{Depleted front interface} \end{cases} \quad (5.24)$$

where

$$\zeta = \frac{1-F(T_{si}/2)}{F(T_{si}/2)} = \left|\frac{dV_{THB}}{dV_{FG}}\right| \quad (5.25)$$

corresponds to the "back coupling coefficient" defined as the slope (in absolute value) of $V_{THB}(V_{FG})$ characteristic for a depleted front interface [7], [10].

From the proposed model for the threshold voltage in vertical DG SOI FinFETs, we can analyze the effect of coupling effect on the threshold voltage:

— The threshold voltage is a constant when the opposite gate is biased in accumulation or strong inversion mode.

— Only for a depleted back or front back interface, the threshold voltage for front- or back-gate varies linearly with V_{BG} or V_{FG}. The slope (in absolute value) of $V_{THF}(V_{BG})$ or $V_{THB}(V_{FG})$ curves of a depleted back or front interface is defined as the "front coupling coefficient" or "back coupling coefficient".

The comparison of our model with the simulated front/back gate threshold voltages as a function of the back/front-gate biases is shown in Figure 5.8. All the threshold voltages were extracted from the conventional Y-function [9]. An overall agreement between the analytical model and simulated results can be observed. With an accumulated back interface (V_{BG} < −20 V in Figure 5.8a), the threshold voltage for

front-channel is constant. With larger V_{BG}, the back interface is depleted and therefore the threshold voltage for front-gate decreases linearly with V_{BG}. The same trend is observed in $V_{THB}(V_{FG})$ curve (Figure 5.8b).

For narrower fin width, the front coupling coefficient λ is smaller whereas the back coupling coefficient ζ is higher. This corresponds to the experimental result shown in Figure 5.4. Furthermore, based on the continuity of threshold voltage, we can derive the intersection points. A and B in Figure 5.8 are ($2\phi_F - V_{FBB}$, $2\varphi_F - V_{FBF}$) and ($2\varphi_F - V_{FBF}$, $2\varphi_F - V_{FBB}$), respectively. They are independent of the geometric parameters, also shown in Figure 5.4. These intersection points symbol the starting of inversion. No plateau corresponding to strong inversion is observed for high positive back-gate or front-gate voltage.

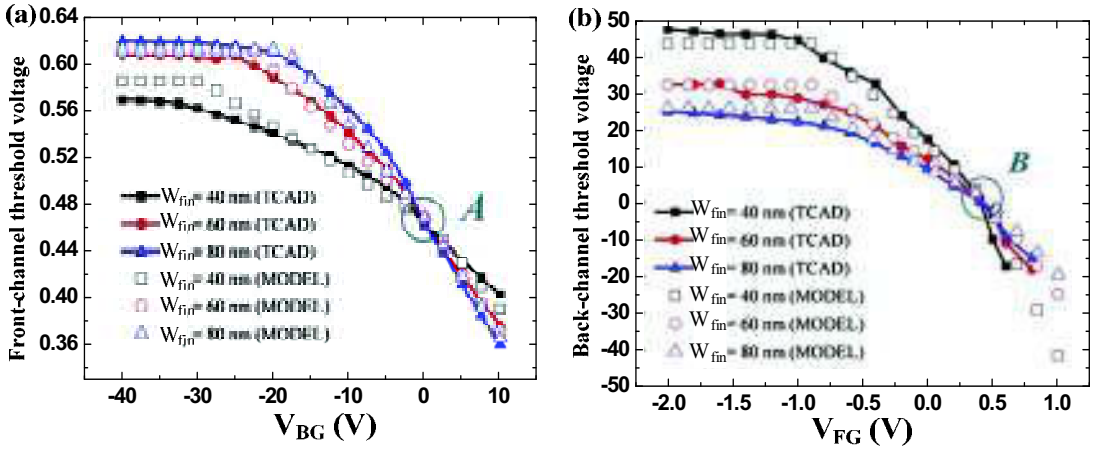

Figure 5.8: *Coupling effects for various fin widths: (a) front-gate threshold voltage versus back-gate bias and (b) back-gate threshold voltage versus front-gate bias.*

Until here, we have systematically investigated the coupling effect in vertical DG SOI FinFETs. The proposed 2D model, used to analyze the effect of coupling effect on the threshold voltage, is an extension of coupling model for triple-gate SOI FinFETs derived by Akarvardar *et al* [10]. However, this initial model only involves the inversion-mode SOI FinFET with undoped or low-doped channel. In next section, we will try to adapt the model to junctionless SOI FinFETs (heavily-doped channel).

2. Coupling effects in junctionless SOI FinFET

Since their invention, junctionless (JL) transistors, especially JL multiple-gate transistors, have been an attractive choice for ultra-scaled devices due to their excellent electrostatic gate control and simplified junction engineering [16]–[18]. Several models based on the approximated solution of the Poisson equation have been proposed: one-dimensional (1D) model for double-gate JL devices [19]–[21], 1D potential model in full depletion region for double-gate JL transistors [22], 2D surface-potential-based current model for triple-gate transistors [23], *etc.* While 2D models are too complicated to be used for parameters extraction, 1D model does not consider the coupling effects between the gates [24]. Therefore, a simple model including coupling effect between gates is imperative for parameters extraction in JL SOI FinFETs. Since we have previously validated the 2D model of potential distribution for inversion-mode vertical DG FinFETs, we will try to modify it for JL SOI FinFETs. Before that, we will firstly show the simulated characteristics of JL SOI FinFETs and the impacts of fin width, film thickness and back-gate.

2.1 TCAD simulations

2.1.1 Simulation set-up

Figure 5.9 shows the simulated structure for an n-channel JL SOI FinFET. The Si film thickness is 9 nm. The thicknesses of gate oxide and BOX are respectively 1.2 nm and 145 nm. The channel has a high arsenic doping concentration (~ 10^{19} cm^{-3}). In order to reduce the access resistance, the source and drain are heavily-doped with arsenic (10^{20} cm^{-3}). The back-gate contact is directly placed on bottom of BOX in order to omit the effect of substrate depletion. The gate length is fixed as 200 nm to avoid short-channel effects. The width of channel varies from 7 nm to 100 nm.

Synopsys Sentaurus TCAD is employed for all simulations [12]. Fermi-Dirac distribution is employed due to heavily-doped channel. The effect of doping, temperature and screen effect are considered, Velocity saturation and the surface scattering are considered by the addition of *Canali* and *Enormal* models. The Shockley-Read-Hall recombination dependent on doping level and Auger recombination are also included. The work-functions of the front- and back-gate are selected to make the flat-band voltages (V_{FBF} and V_{FBB}) equal to zero. The drain is 0.05 V and the gate is swept from −1.5 V to +1.5 V.

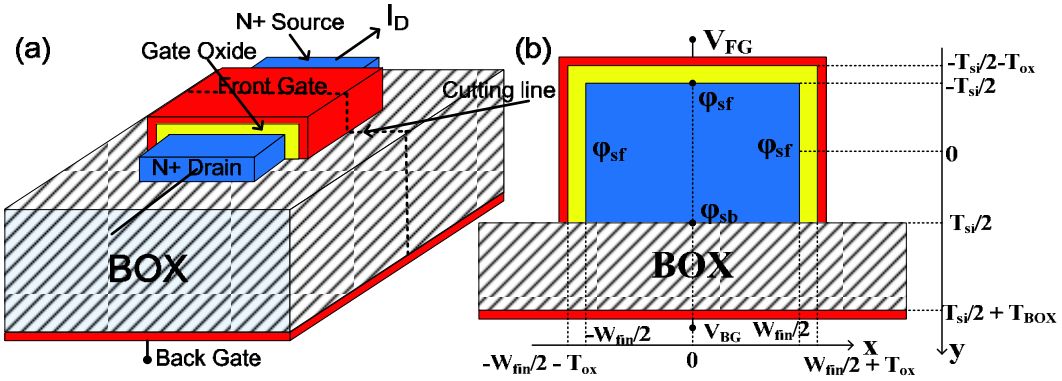

Figure 5.9: *(a) The schematic structure and (b) cross-section for simulated n-channel JL SOI FinFETs.*

2.1.2 Simulated results

- **Characteristic curves**

Figure 5.10 shows the simulated drain current and transconductance for JL SOI FinFETs with different fin width. For V_{FG} = 0 V (corresponding to flat-band), the drain current is significant due to volume conduction. At higher front-voltage, the drain current increases further as a result of an activated accumulation channel under the front-gate. For V_{FG} < 0 V, the current decreases until the channel is fully depleted (~ −1.1 V for W_{fin} = 100 nm, where a sharp decrease of drain current is observed in the semi-logarithmic scale of Figure 5.10a).

These modes of operation are also reflected by the contours of electron densities in Figure 5.11. For V_{FG} = V_{FBF} (input value is 0 V), the drain current equals to the volume current (Figure 5.11a). The junctionless transistors can work in three modes:

1) In accumulation mode (V_{FG} > V_{FBF}), the drain current is the sum of volume current and accumulation current (Figure 5.11b);
2) In partial depletion mode, the drain current comes from the volume conduction in the undepleted region (Figure 5.11c);
3) In full depletion mode, the drain current decreases sharply with V_{FG} (Figure 5.11d).

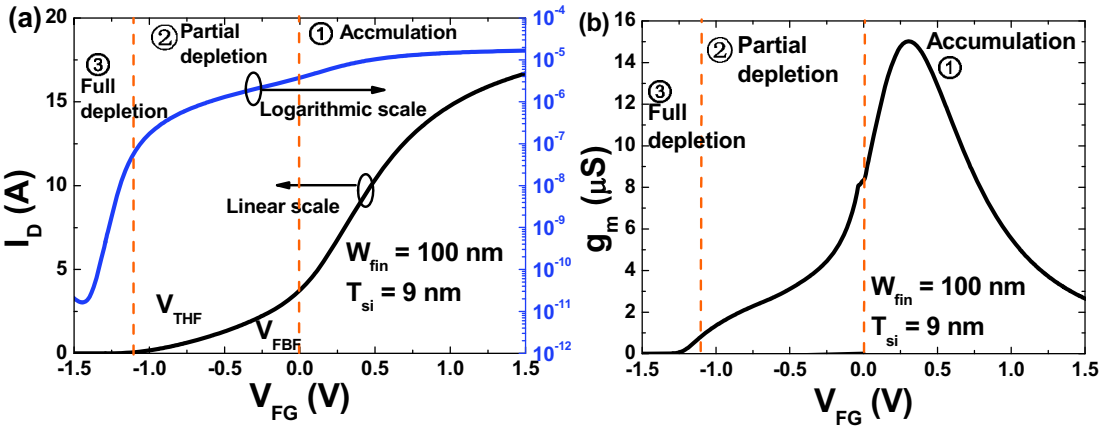

Figure 5.10: *(a) Simulated drain currents and (b) transconductance versus front-gate voltage for wide JL SOI FinFETs. $N_D = 10^{19}$ cm^{-3}, T_{si} = 9 nm, V_D = 0.05 V and V_{BG} = 0 V.*

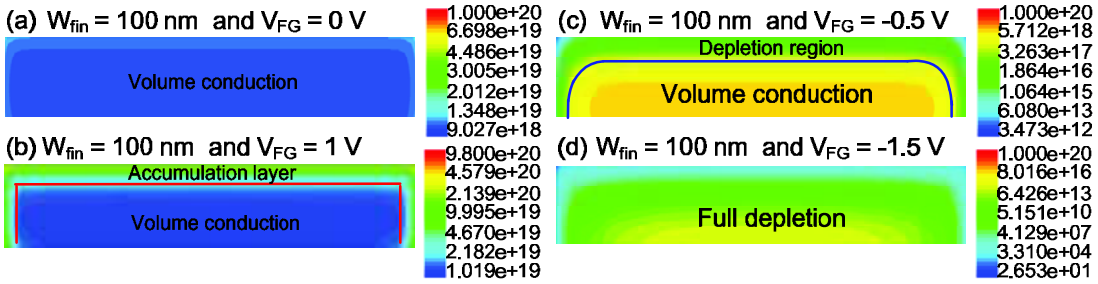

Figure 5.11: *Electron density profiles for (a) only volume conduction, (b) accumulation, (c) partial depletion and (d) full depletion. $N_D = 10^{19}$ cm^{-3}, T_{si} = 9 nm, V_D = 0.05 V and V_{BG} = 0 V.*

- **Effect of fin width and film thickness**

The effect of fin width on the transconductance curves $g_m(V_{FG})$ is shown in Figure 5.12a. For wide fin (W_{fin} = 100 nm), a plateau appears in the partially-depleted region (−1.1 V < V_{FG} < 0 V) due to the volume conduction. With the fin width decreasing, the g_m plateau reduces until it disappears. This can be attributed to the enhanced control of lateral-gates for narrower devices. The effect of film thickness was also simulated, as shown in Figure 5.12b. For a narrow fin (W_{fin} = 9 nm), g_m shifts negatively with increasing film thickness due to the reduced control of top-gate. The transconductance and current are obviously lighter if one dimension of the fin (width or thickness) increases. The other dimension should be small enough to guarantee device turn-off.

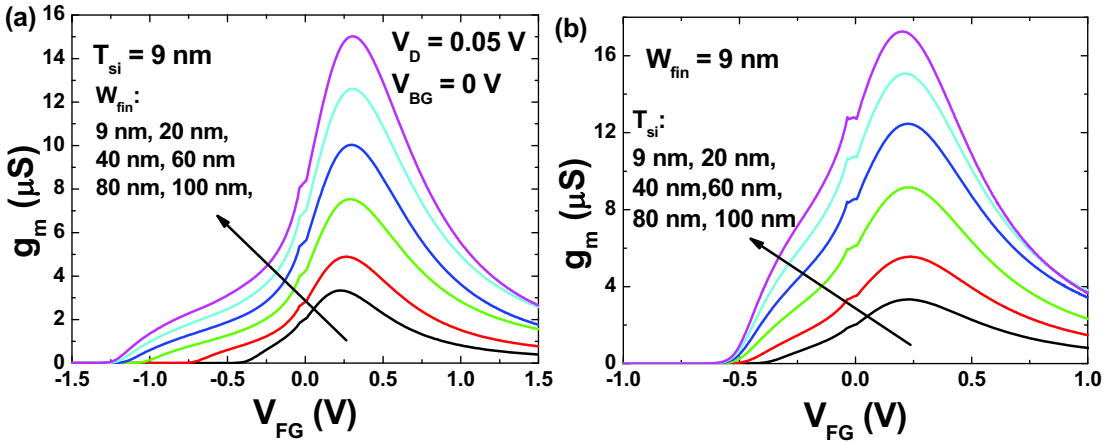

***Figure 5.12**: Effect of (a) fin width and (b) film thickness on thin JL SOI FinFET. $N_D = 10^{19}$ cm^{-3}, V_D = 0.05 V and V_{BG} = 0 V.*

- **Effect of back-gate**

Figure 5.13a compares the drain current of a wide JL SOI FinFET with different back-gate bias. For positive back-gate, the drain current shifts negatively and is higher due to the formation of accumulation channel on the Si/BOX interface. For $V_{BG} < 0$ V, the back channel is simply depleted (strong inversion would be obtained for $V_{BG} <$ −80 V according to Eq (2. 16)), and therefore the drain current decreases. For narrow JL SOI FinFET, the effect of back-gate on the drain current weakens due to the domination of lateral-gates, as shown in Figure 5.13b.

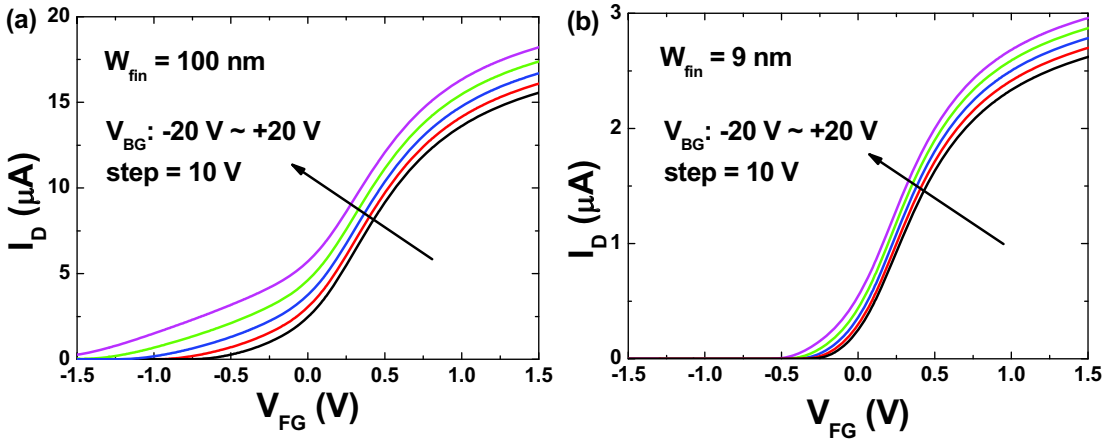

***Figure 5.13:** Effect of back-gate on the drain currents for: (a) wide and (b) narrow JL SOI FinFETs. $N_D = 10^{19}$ cm^{-3}, T_{si} = 9 nm and V_D = 0.05 V.*

This suppression of coupling effect between top- and back-gates is also visible in the comparison of $I_D(V_{FG})$ curves under different back-gate bias (Figure 5.14). For wide JL SOI FinFET, g_m strongly varies with V_{BG} only in partial depletion mode, but

almost keeps unchanged in accumulation mode; for narrow JL FinFET, the variation of g_m with V_{BG} reduces. This is similar to the effect of fin width on the coupling effect between top- and back-gates in inversion-mode SOI FinFETs (Figure 5.2). For a narrow and tall JL SOI FinFET, the lateral-gates completely control the channel and therefore the coupling between top- and back-gate has smaller impact, as shown in Figure 5.15.

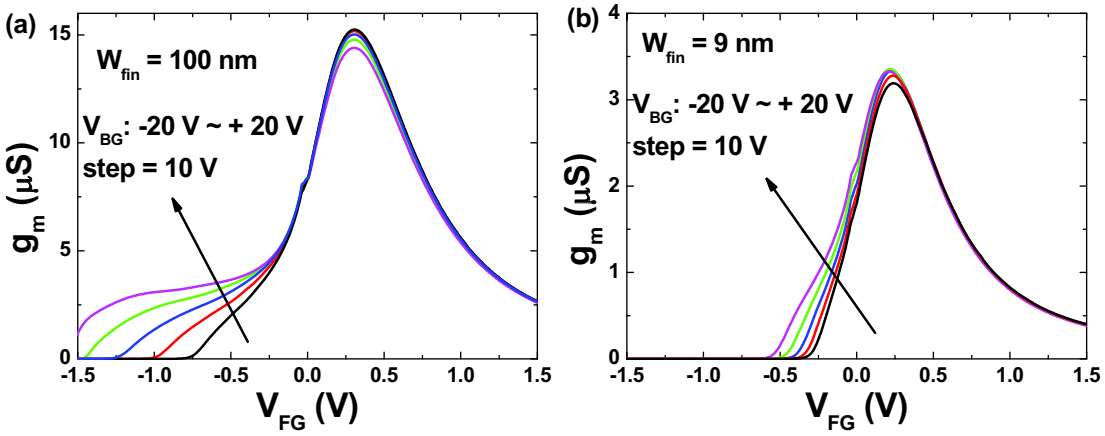

***Figure 5.14**: Effect of back-gate on the transconductance for: (a) wide and (b) narrow JL SOI FinFETs. $N_D = 10^{19}$ cm^{-3}, T_{si} = 9 nm and V_D = 0.05 V.*

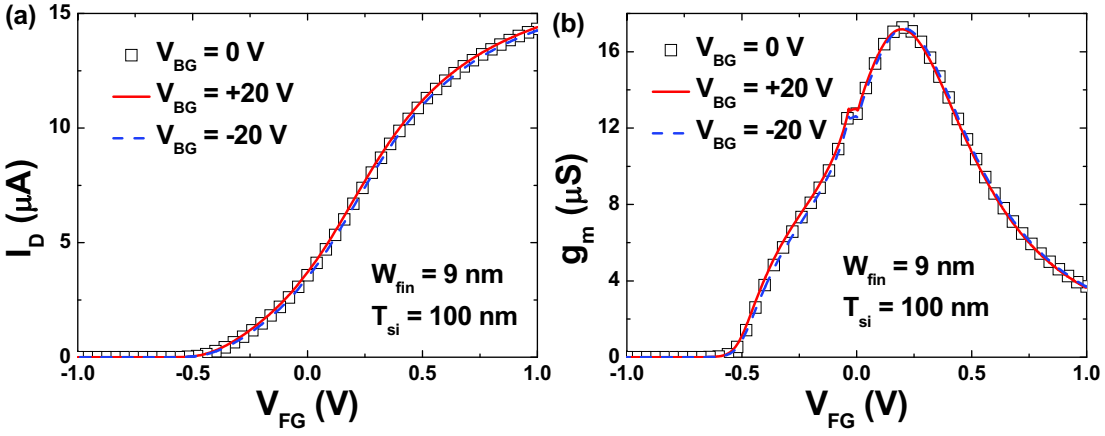

***Figure 5.15:** Effect of back-gate on narrow and tall JL SOI FinFET for: (a) $I_D(V_{FG})$ and (b) $g_m(V_{FG})$ The coupling effect fully connected. $N_D = 10^{19}$ cm^{-3}, V_D = 0.05 V and V_{BG} = 0 V.*

In conclusion, the coupling effect in JL SOI FinFETs plays the same role as in the inversion-mode vertical DG SOI FinFETs discussed in the previous section:

— With the fin width decreasing, the coupling effect between top- and back-gates weakens.

— With the film thickness increasing, the effect of top-gate reduces.

— For a narrow fin, the device is mainly governed by the lateral-gates.

Therefore, the 2D analytical model of potential distribution for the inversion-mode SOI FinFETs might be adapted to the JL SOI FinFETs. Next sub-section describes the modifications needed and the results.

2.2 Modeling of 2D potential distribution in full depletion mode

2.2.1 Description of 2D potential model

Different from the inversion-mode SOI FinFETs, the channel for JL SOI FinFETs is heavily-doped (~ 10^{19} cm^{-3}). Therefore, the 2D Laplace equation (Eq. (5.6)) fails to model the potential distribution due to the fixed charge that cannot be neglected in the full depletion region. Thus, the 2D Poisson's equation for an n-channel junctionless FinFET is given by:

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = -\frac{qN_D}{\varepsilon_{si}} \tag{5.26}$$

According to [10], the potential between the two lateral-gates is still parabolic in the JL SOI FinFETs. Therefore, the 2D potential in JL SOI FinFETs has the same shape as in inversion-mode vertical DG SOI FinFETs (Eq. (5.5)). Substituting Eq. (5.5) into Eq. (5.26) and letting $x = 0$, Eq. (5.7) is rewritten as:

$$\frac{d^2 \varphi(0,y)}{dy^2} - \frac{1}{W_0^{\,2}} \varphi(0,y) + \left(\frac{V_{FG} - V_{FBF}}{W_0^{\,2}} + \frac{qN_D}{\varepsilon_{si}} \right) = 0 \tag{5.27}$$

Considering boundary conditions between silicon and silicon dioxide (gate oxide and BOX), the solution of Eq. (5.27) has the form of:

$$\varphi(0,y) = C_3 \sinh\left(\frac{y}{W_0}\right) + C_4 \cosh\left(\frac{y}{W_0}\right) + V_{FG} - V_{FBF} + \frac{qN_D W_0^{\,2}}{\varepsilon_{si}} \tag{5.28}$$

Here, C_3 and C_4 are the coefficients determined by the boundary conditions of the top ($y = -T_{si}/2$) and bottom ($y = T_{si}/2$) interfaces. Note that the thickness of top-gate oxide is equal to that of lateral-gates oxide in the modeled triple-gate JL transistor ($T_{tox} = T_{lox} = T_{ox}$). Substituting Eq. (5.28) into Eqs. (5.9) and (5.10), we calculate C_3 and C_4 as:

$$C_3 = \left(V_{BG} - V_{FBB} - V_{FG} + V_{FBF} - \frac{qN_D W_0^2}{\varepsilon_{si}} \right) \cdot \frac{\cosh\left(T_2 / W_0\right)\cosh\left[(T_{si}/2 + T_1)/W_0\right]}{\sinh\left[(T_{si} + T_1 + T_2)/W_0\right]} + \frac{qN_D W_0^2}{\varepsilon_{si}} \cdot \frac{\cosh\left(T_1 / W_0\right)\cosh\left[(T_{si}/2 + T_2)/W_0\right]}{\sinh\left[(T_{si} + T_1 + T_2)/W_0\right]}$$

$$C_4 = \left(V_{BG} - V_{FBB} - V_{FG} + V_{FBF} - \frac{qN_D W_0^2}{\varepsilon_{si}} \right) \cdot \frac{\cosh\left(T_2 / W_0\right)\sinh\left[(T_{si}/2 + T_1)/W_0\right]}{\sinh\left[(T_{si} + T_1 + T_2)/W_0\right]} - \frac{qN_D W_0^2}{\varepsilon_{si}} \cdot \frac{\cosh\left(T_1 / W_0\right)\sinh\left[(T_{si}/2 + T_2)/W_0\right]}{\sinh\left[(T_{si} + T_1 + T_2)/W_0\right]} \tag{5.29}$$

where

$$T_1 = W_0 ar\tanh\eta_1 = W_0 ar\tanh\left(\frac{\varepsilon_{si}}{C_{lox}W_0}\right) = W_0 ar\tanh\left(\frac{\varepsilon_{si}}{C_{ox}W_0}\right) \tag{5.30}$$

$$T_2 = W_0 ar\tanh\eta_2 = W_0 ar\tanh\left(\frac{\varepsilon_{si}}{C_{BOX}W_0}\right) \tag{5.31}$$

W_0 represents the equivalent fin width when the channel is controlled by top- and back-gates ($\eta_0 = \varepsilon_{si}/C_{lox}W_{fin} = C_{fin}/C_{lox}$ and $W_0 = \sqrt{1/8 + \eta_0/2}\cdot W_{fin}$.). Therefore, Eq. (5.28) can be rewritten as:

$$\varphi(0,y) = \left(V_{BG} - V_{FBB} - V_{FG} + V_{FBF} - \frac{qN_D W_0^2}{\varepsilon_{si}} \right) \cdot \frac{\cosh\left(T_2 / W_0\right)\sinh\left[(y + T_{si}/2 + T_1)/W_0\right]}{\sinh\left[(T_{si} + T_1 + T_2)/W_0\right]} - \frac{qN_D W_0^2}{\varepsilon_{si}} \cdot \frac{\cosh\left(T_1 / W_0\right)\sinh\left[(T_{si}/2 - y + T_2)/W_0\right]}{\sinh\left[(T_{si} + T_1 + T_2)/W_0\right]} + V_{FG} + V_{FBF} + \frac{qN_D W_0^2}{\varepsilon_{si}} \tag{5.32}$$

Substituting Eq. (5.28) into Eq. (5.5), the 2D potential distribution for an n-channel JL SOI FinFET is obtained analytically.

2.2.2 Validation by simulations

In order to validate our model for the potential distribution in JL SOI FinFET, we compare $\varphi(0, y)$, the potential of full depletion region along $x = 0$ (vertical cut in the middle of the channel), between model and simulations, as shown in Figure 5.16. For both wide (Figure 5.16a) and narrow (Figure 5.16b) JL SOI FinFETs, the modeled potentials follow the variation of simulated potential with front-gate voltage. However, in partial depletion region, the modeled potentials deviate from the simulated ones, as

shown in Figure 5.17. This confirms that our model is valid and useful in full depletion regime where the hypothesis in Eq. (5.26) is correct.

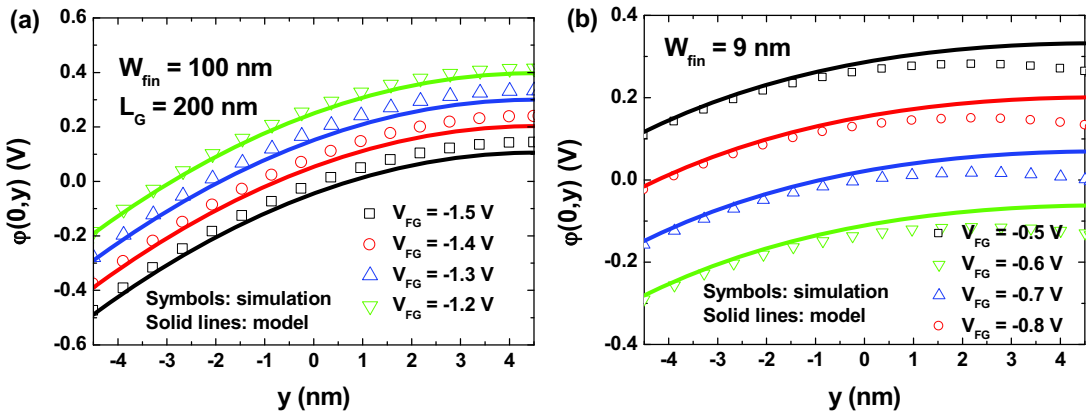

Figure 5.16: *Potential profiles in full depletion region along $x = 0$ as functions of the front-gate voltage for: (a) wide JL SOI FinFET (W_{fin} = 100 nm) and a narrow JL SOI FinFET (W_{fin} = 9 nm). $N_D = 10^{19}$ cm^{-3}, T_{si} = 9 nm, V_D = 0.05 V and V_{BG} = 0 V. $y = -T_{si}/2$ is at the top of the film and $y = T_{si}/2$ is at the BOX interface.*

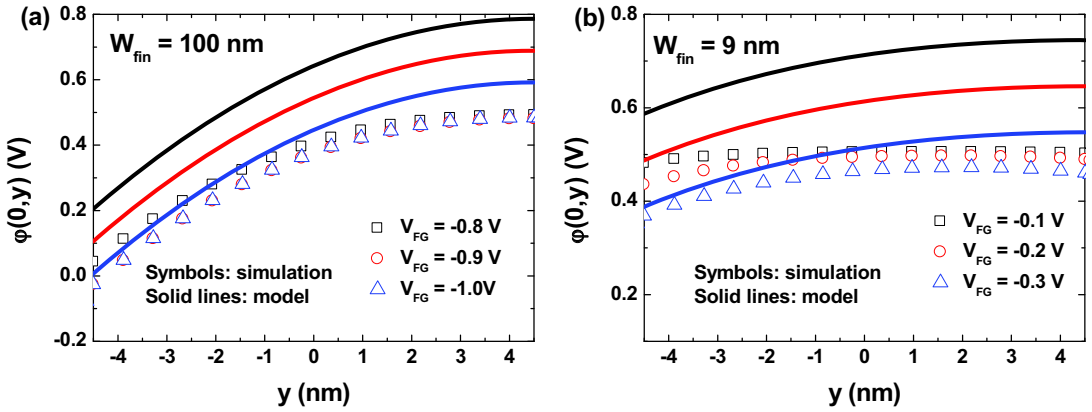

Figure 5.17: *Potential profiles in partially-depleted region along $x = 0$ for variable front-gate voltage. (a) W_{fin} = 100 nm and (b) W_{fin} = 9 nm. $N_D = 10^{19}$ cm^{-3}, T_{si} = 9 nm, V_D = 0.05 V and V_{BG} = 0 V.*

The effect of back-gate on the potential in both wide and narrow JL SOI FinFETs is shown in Figure 5.18. For wide devices, an accumulation layer is formed when back-gate is positively biased (squares and circles in Figure 5.18a), leading to the failure of full depletion approximation. More negative front-gate bias ($V_{FG} < -1$ V) is needed to obtain full depletion. When the channel at the bottom is depleted ($V_{BG} = -10$ & -20 V), the modeled potential (circles and squares in Figure 5.18a) shows excellent agreement with the simulated ones. Compared to the wide devices, the effect of back-gate on the body potential in narrow JL SOI FinFETs is minor since the channel is

mainly controlled by the lateral-gates. However, the accumulation layer triggered by the positive back-gate bias still leads to a small deviation at the bottom of the channel (y = 4.5 nm), as shown in Figure 5.18b.

In summary, this 2D potential model works in full depletion regime with zero back-gate bias or with $V_{BG} < 0$ V (depletion at back interface).

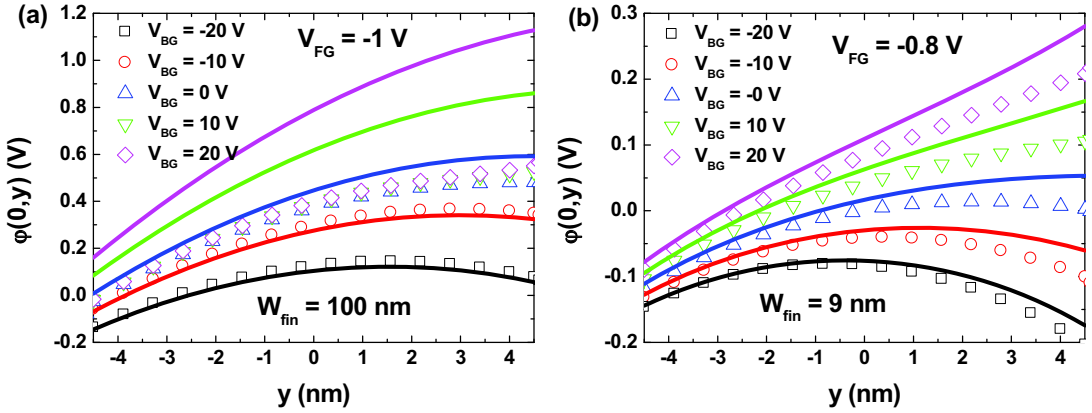

Figure 5.18: *Potential profiles in full depletion region along x = 0 as the functions of back-gate voltages for devices with (a) W_{fin} = 100 nm and (b) W_{fin} = 9 nm. $N_D = 10^{19}$ cm^{-3} and T_{si} = 9 nm.*

2.2.3 Applications of 2D potential model

Since our 2D potential model applies to the full depletion region of nano-channel JL SOI FinFETs, we can use it to extract the threshold voltage, which is a key identifier to distinguish the full and partial depletion regions. Before using the model, we will introduce the current-voltage method proposed by Jeon *et al.* [25] to extract threshold voltage.

- **Conventional method to extract threshold voltage**

In planar junctionless transistors, threshold voltage is determined from the derivative of the transconductance (dg_m/dV_{FG}), shown in Figure 5.19 [25]. The first peak P_1 corresponds to flat-band voltage, where the channel of the junctionless transistor is just changed from surface accumulation to neutral state; the second peak P_2 exhibits the threshold voltage, separating the partial and full depletion regions (dotted line in Figure 5.19a). This method works in wide junctionless SOI FinFET (square in Figure 5.19a), but fails in narrow JL SOI FinFETs where the coupling effect from lateral-gates is extremely strong. As shown in Figure 5.19b for narrower fin, the two peaks

trend to merge together, leading to difficulty in determination of threshold voltage and flat-band voltage. On the other hand, the experiments have demonstrated that high access resistance would lead to the disappearance of P_2 [25], also making the threshold voltage extraction impossible.

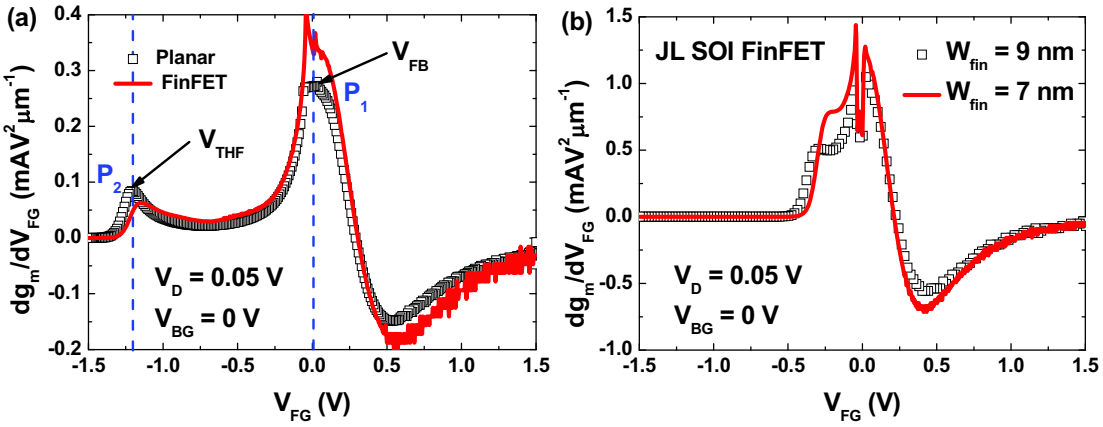

Figure 5.19: *(a) Simulated dg_m/dV_{FG} versus V_{FG} for a planar Si JL transistor and a wide JL SOI FinFET (W_{fin} = 100 nm); (b) simulated dg_m/dV_{FG} versus V_{FG} for two nano-channel junctionless SOI FinFETs (W_{fin} = 9 nm and 7 nm). T_{si} = 9 nm, L_G = 200 nm and $N_D = 10^{19}$ cm^{-3}.*

- **Extraction of threshold voltage from the 2D potential model**

According to [22], the threshold voltage V_{THF} for junctionless transistors can be defined as the front-gate voltage when the channel is just fully depleted. It is given as the maximum potential at $(x, y) = (0, -T_{si}/2)$ for V_{BG} = 0 V from Eq.(5.32), which corresponds to the point depleted at last. Therefore, we have:

$$\left.\frac{\partial\varphi(0,y)}{\partial y}\right|_{y=-\frac{T_{si}}{2}\ and\ V_{FG}=V_{THF}} = 0 \tag{5.33}$$

Substituting Eq. (5.28) into Eq. (5.33), the threshold voltage of front-gate can be modeled as:

$$V_{THF} = \frac{qN_D W_0^{\,2}}{\varepsilon_{si}} \cdot \frac{\cosh(T_1/W_0)\sinh(T_2/W_0) - \cosh(T_2/W_0)\cosh\left[(T_{si}+T_1)/W_0\right]}{\cosh(T_2/W_0)\cosh\left[(T_{si}+T_1)/W_0\right]} + V_{FBF} \tag{5.34}$$

With fin width shrinking, the control of lateral-gates on the channel enhances, so the threshold voltage of front-channel shifts closer to the flat-band voltage (V_{FBF} = 0 V), as shown in Figure 5.20a. The threshold voltage calculated from Eq. (5.34) coincides

with the one extracted from the dg_m/dV_{FG} (Figure 5.20b) [25]. The deviation for wide fin (W_{fin} > 30 nm) can possibly be attributed to the effect of mobile charge. With wider fin, the mobile charge density is larger for $V_{FG} = V_{THF}$, leading to the imperfection of full depletion approximation (see the large subthreshold current for wide JL in Figure 5.10a)

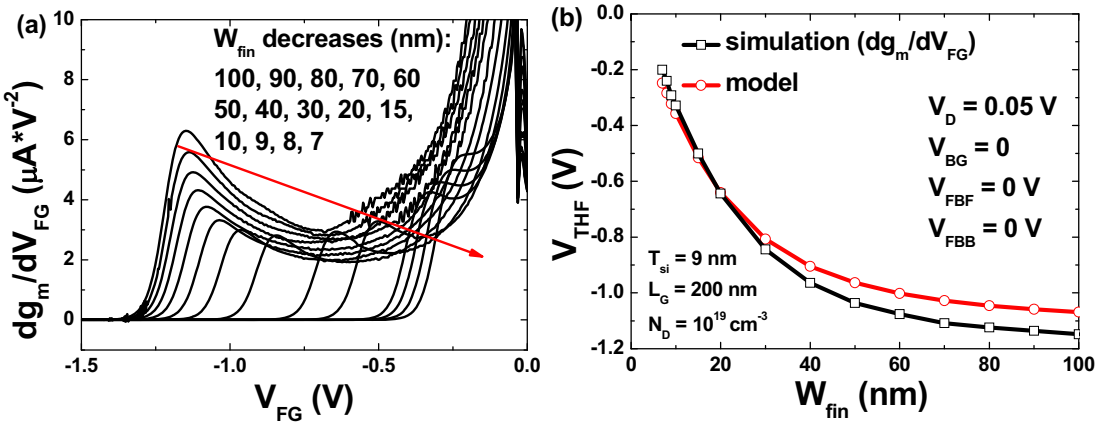

Figure 5.20: *(a) Simulated dg_m/dV_{FG} versus V_{FG} and (b) threshold voltage of front-gate for different fin width extracted from Eq. (5.34) and the second peak of dg_m/dV_{FG}.*

For depletion at back channel, the point y_m depleted at last lies in the middle of the channel along $x = 0$. Assume that the potential at y_m does not vary with V_{FG} and V_{BG} and is always equal to the Fermi potential φ_F. Therefore, we have:

$$\varphi(0, y_m) = \varphi_F = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{5.35}$$

For $V_{FG} = V_{THF}$, the electric field at y_m approximates zero:

$$\left.\frac{\partial \varphi(0, y)}{\partial y}\right|_{y=y_m \text{ and } V_{FG}=V_{THF}} = 0 \tag{5.36}$$

Combining Eqs. (5.35) and (5.36), we can obtain the relationship between y_m and V_{BG}, as shown in Figure 5.21a. For more V_{BG}, y_m shifts from the bottom of the fin toward the top. For narrower fin, stronger depletion is induced by lateral-gates and therefore this shift is larger. The threshold voltage is modeled as:

$$V_{THF} = V_{BG} - V_{FBB} - \frac{qN_D W_0^2}{\varepsilon_{si}} + \frac{\cosh\left(T_1/W_0\right)\cosh\left[\left(T_{si}/2 - y_m + T_2\right)/W_0\right]}{\cosh\left(T_2/W_0\right)\cosh\left[\left(T_{si}/2 + y_m + T_1\right)/W_0\right]} \cdot \frac{qN_D W_0^2}{\varepsilon_{si}} \tag{5.37}$$

Figure 5.21b compares the extracted threshold voltage between dg_m/dV_{FG} method and Eq. (5.37) under different V_{BG}. Our model shows good agreement in particular for nanowires. For wide fin, the threshold voltage increases more negatively, which can be explained by the fact that the back-gate helps to deplete the channel. For narrower fin, the channel is mainly controlled by lateral-gates and therefore the variation of threshold voltage is smaller.

It follows that Eq. (5.37) can be safely used to calculate the threshold voltage for V_{BG} = 0 V or depletion at back interface, if the flat-band voltages for front- and back-gates and the doping concentrations are known from technology.

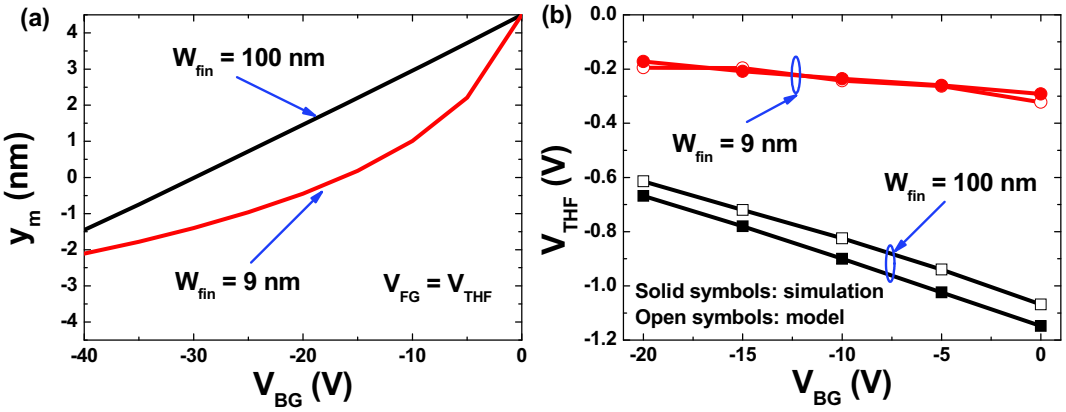

Figure 5.21: *(a) y_m versus V_{BG} and (b) comparison of extracted V_{THF} between dg_m/dV_{FG} method and our model (Eq. (5.37)).*

- **Extraction of channel concentration from 2D potential model**

Once the threshold voltage and flat-band voltage are known, the doping concentration of the channel can be determined. We can rewrite Eq. (5.34) as:

$$N_D = \frac{\varepsilon_{si}}{q \cdot W_0^2} \cdot \frac{\left(-V_{THF} + V_{FBF}\right)\cosh\left(T_2/W_0\right)\cosh\left[\left(T_{si} + T_1\right)/W_0\right]}{\cosh\left(T_2/W_0\right)\cosh\left[\left(T_{si} + T_1\right)/W_0\right] - \cosh\left(T_1/W_0\right)\sinh\left(T_2/W_0\right)} \tag{5.38}$$

Table 5-I summarizes the extracted doping level for different fin width, which shows excellent agreement with the input doping concentration (10^{19} cm^{-3}) for W_{fin} > 10 nm.

For narrower JL FinFETs (W_{fin} < 10 nm), the extracted doping level is a little underestimated.

Table 5-I: Extracted doping level from Eq. (5.38) for different fin width.

W_{fin} (nm)	Extracted N_D (10^{19} cm^{-3})	W_{fin} (nm)	Extracted N_D (10^{19} cm^{-3})
100	1	30	1
90	1	20	1
80	1	15	1
70	1	10	0.92
60	1	9	0.91
50	1	8	0.84
40	1	7	0.81

Conclusions of Part A:

We have modeled the 2D potential distribution for the subthreshold region of operation of vertical DG inversion-mode SOI FinFETs and junctionless SOI FinFETs. Table 5-II summarizes the working range of these two models. The effect of coupling between top- and back-gates on the threshold voltage can be predicted in inversion-mode FinFETs. As Table 5-II shows, for JL SOI FinFETs, this model cannot work in partial depletion and surface accumulation regimes. For this reason, we will focus on these two regimes in part B.

***Table 5-II:** Working range of 2D potential model in inversion-mode and junctionless FinFETs.*

Device type	States of back or front interface		
	Channel OFF	Transition	Channel ON
Vertical DG inversion- mode SOI FinFETs	Accumulation	Partial depletion	Inversion
JL SOI FinFETs	Full depletion	×	×

Part B: Modeling of junctionless SOI FinFETs for parameters extraction

In this part, we will propose an alternative modeling of JL transistors in order to extract parameters from $I_D(V_G)$ curves. Since the full depletion region was contained in part A, we will discuss the partial depletion region in section 2.3 and the accumulation region in section 2.4.

2.3 Modeling of carrier profile in partial depletion mode

2.3.1 Description and validation of carrier density model

In partially-depleted region, the operation of JL devices relies on the expansion of the depletion regions triggered by each gate until they cut off the volume conductance. It is therefore important to model the carrier profile in the partial depletion region. In n-doped JL transistor, the extension of 1D depletion width (W_D) with V_{FG} governs the volume conductance and the drain current [20]:

$$W_D = \frac{\varepsilon_{si}}{C_{OX}}\left(-1+\sqrt{1-\frac{2C_{OX}^{\ 2}}{qN_D\varepsilon_{si}}\left(V_{FG}-V_{FBF}-V^*\right)}\right) \tag{5.39}$$

where V^* is a reference potential used to adjust the fitting curves [26]. According to Eq. (5.39), the width of the depletion region in thick planar MOS structures increases when V_{FG} is more negative (solid lines in Figure 5.22). For comparison, we used W_D values extracted from TCAD simulations. The simulated width of the depletion region is defined by the point where the carrier concentration equals half of the doping level (as will be explained in section 2.3.2). The calculated W_D follows well the simulated values (open symbols in Figure 5.22) for a large interval of V_{FG} before saturation. Note that the saturation of simulated W_D values corresponds well to W_{Dmax} (maximum width of depletion region), given by Eq. (2.16). Table 5-III summarizes the W_{Dmax} for three dopant concentrations, used in Figure 5.22.

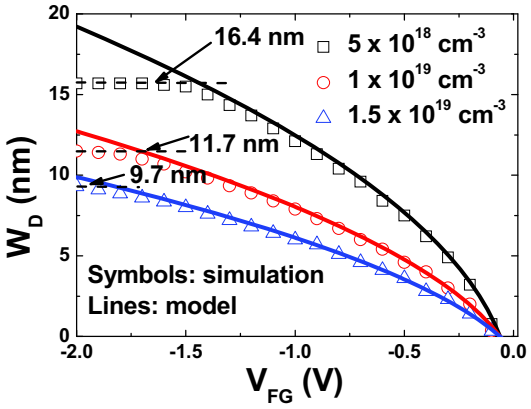

Figure 5.22: *Simulated depletion depth versus gate bias in planar JL FET. T_{si} = 50 nm.*

Table 5-III: *Maximum width of depletion region.*

N_D (cm^{-3})	5×10^{18}	10^{19}	1.5×10^{19}
W_{Dmax} (nm)	16.4	11.7	9.7

Based on the width of depletion region (W_D) and doping level (N_D), we will develop a simple model of carrier profile for three configurations: single-gate (SG), double-gate (DG) and triple-gate (TG) JL.

— **Wide SG JL:** only the top-gate is turned on and both side gates are biased at flat-band voltage V_{FBF} (Figure 5.23a);

— **Tall DG JL:** the lateral-gates are connected together and the top-gate is biased at V_{FBF} (Figure 5.23b);

— **TG JL:** three gates are connected and turned on together (Figure 5.23c).

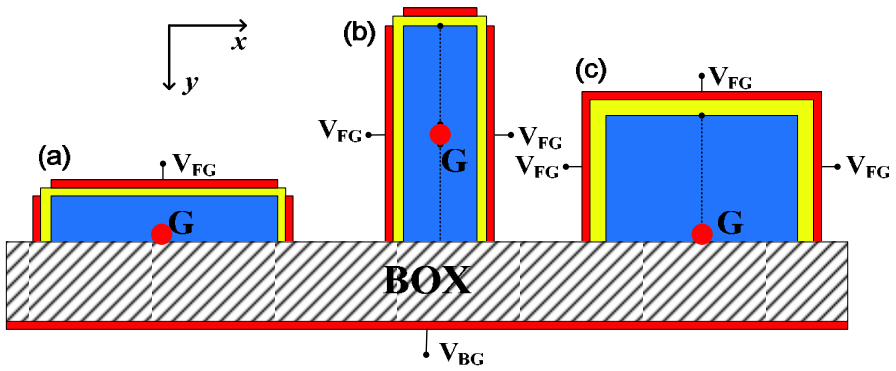

Figure 5.23*: Three configurations for JL FinFETs: (a) SG, (b) DG and (c) TG. (0,0) point locates at the center of the body.*

- **SG JL**

In this configuration, the channel is only controlled by the top-gate (Figure 5.23a). Most JL models account for an abrupt boundary between neutral and depleted regions. In fact, the majority carrier profile exhibits a gradual variation, governed by the Debye length. Allibert *et al.* [27] have proposed an empirical function to explain the smooth transition from partial to full depletion in SOI devices. Adapting this empirical function to SG JL transistors we obtain the majority carrier profile:

$$N^*(y) = \frac{N_D}{2}\left(1 + tanh\left(\frac{y + T_{si}/2 - W_D}{\alpha L_D}\right)\right) \tag{5.40}$$

where L_D is Debye length ($L_D = \sqrt{\frac{\varepsilon_{si} kT}{q^2 N_D}}$) and α is a fitting factor ($\alpha \approx 1.7$) [27]. For thick SG JL devices (T_{si} = 50 nm, Figure 5.24a), various V_{FG} were simulated and the model (solid lines) matches perfectly the simulated curves (open symbols). For thin SG JL devices (T_{si} = 9 nm, Figure 5.24b), the agreement is also good, except for very small carrier densities at the bottom interface ($V_{FG} \leq -0.7$ V where the device starts to work in subthreshold region). Nevertheless, our model still follows the variation of the simulated carrier density at the bottom. Different doping and thickness values were also successfully tested, as shown in Figure 5.25.

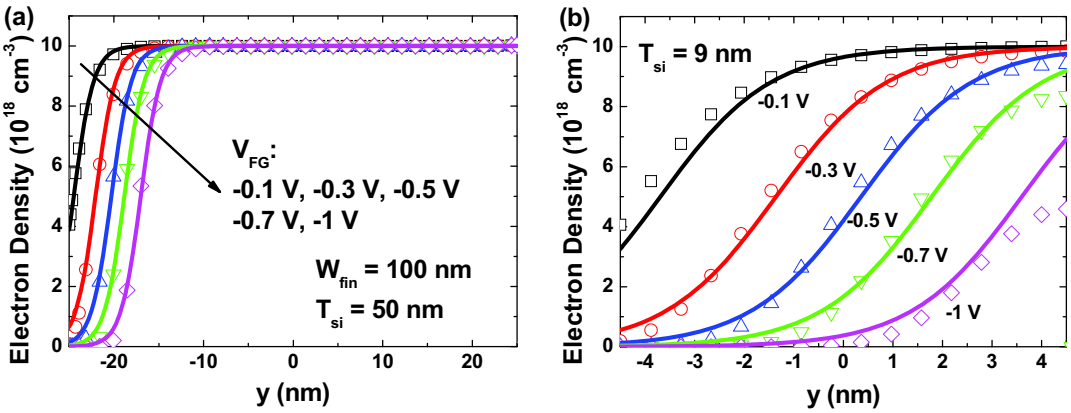

Figure 5.24: *Comparison of carrier profiles for single-gate JL transistors with $N_D = 10^{19}$ cm^{-3}: (a) T_{si} = 50 nm and (b) T_{si} = 9 nm. W_{fin} = 100 nm and L_G = 200 nm. V_{BG} = 0 V.*

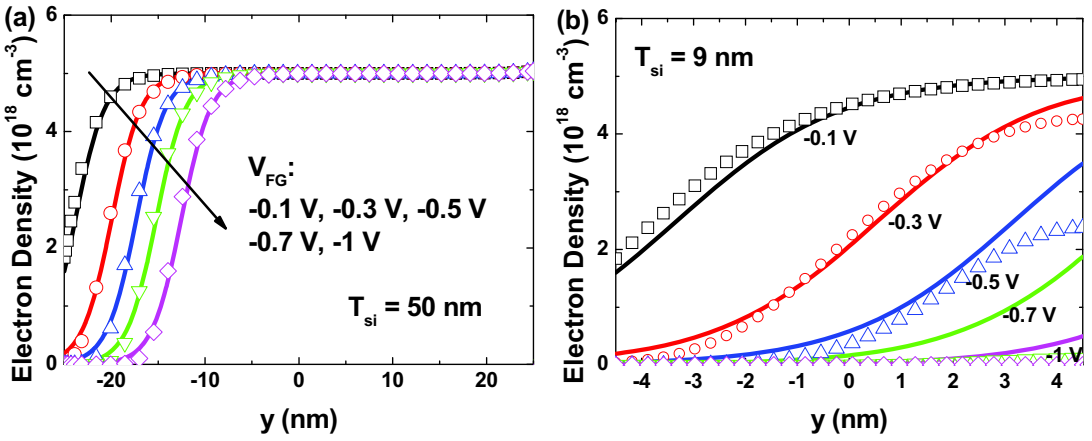

Figure 5.25: *Comparison of carrier profiles for single-gate junctionless transistors with $N_D = 5 \times 10^{18}$ cm^{-3}: (a) $T_{si} = 50$ nm and (b) $T_{si} = 9$ nm. $W_{fin} = 100$ nm and $L_G = 200$ nm. $V_D = 0.05$ V and $V_{BG} = 0$ V. Model: solid lines; Simulation: open symbols.*

The threshold voltage is defined when the depletion region reaches the bottom of the body (G-point, Figure 5.23a), in other words when the maximum concentration of majority carriers becomes $N^*(T_{si}/2) = N_D/2$. When the carrier density at G-point is lower than $N_D/2$, the channel is fully depleted (subthreshold region, not accounted for by our model). The same criterion ($N_D/2$) for the carrier density was used to determine the simulated width of depletion region in a thick MOS structure (open symbols in Figure 5.22).

- **DG JL**

The device is driven by lateral-gates (Figure 5.23b). Both depletion regions expand concomitantly with V_{FG} decreasing. In this case, we assume that one gate acts on the 'effective' doping defined by the opposite gate. Applying Eq. (5.40) to the lateral-gates and replacing N_D seen by one gate with the carrier profile governed by the opposite gate, yields the carrier profile for DG JL:

$$N^*(x) = \frac{N_D}{4}\left(1+\tanh\left(\frac{x+W_{fin}/2-W_D}{\alpha L_D}\right)\right)\cdot\left(1+\tanh\left(\frac{-x+W_{fin}/2-W_D}{\alpha L_D}\right)\right) \quad (5.41)$$

The modeled carrier profiles show very good agreement with the 3D simulations for wide DG JL devices (Figure 5.26a). In extremely narrow DG JL transistors (Figure 5.26b), our model matches well with the simulations only for larger V_{FG} (≥ -0.3 V); for more negative V_{FG}, a deviation appears at the center of the channel which enters

the subthreshold region. Similar to SG JL, we define a criterion for the carrier density at G-point (Figure 5.23b) to distinguish the partial and full depletion for DG JL. The two depletion regions meet each other in the middle of the fin: $W_D = W_{fin}/2$. The threshold voltage is given by the gate voltage for which the carrier density at G-point is: $N^*(0) = N_D/4$.

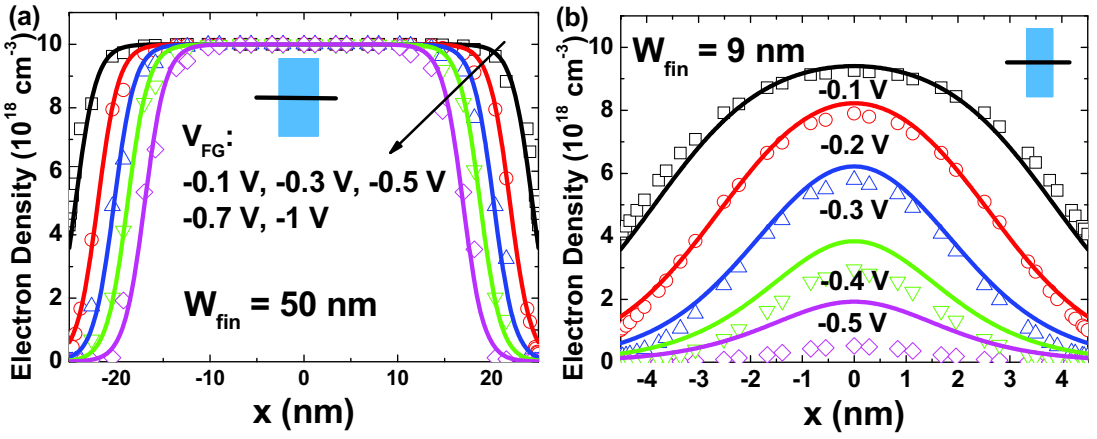

Figure 5.26: *Comparison of carrier profiles in double-gate JL transistors with $N_D = 10^{19}$ cm^{-3}: (a) W_{fin} = 50 nm (partially-depleted) and (b) W_{fin} = 9 nm (fully-depleted). T_{si} = 100 nm and L_G = 200 nm. V_D = 0.05 V and V_{BG} = 0 V. Solid lines: analytical model; open symbols: numerical simulations.*

- **TG JL**

The principle for the modeling of TG JL is the same as in DG JL. The apparent doping induced by top-gate is replacing N_D in Eq. (5.41). The effective doping profile in the body is:

$$N^*(x,y) = \frac{N_D}{8}\left(1+tanh\left(\frac{x+W_{fin}/2-W_D}{\alpha L_D}\right)\right)\cdot\left(1+tanh\left(\frac{-x+W_{fin}/2-W_D}{\alpha L_D}\right)\right)\cdot\left(1+tanh\left(\frac{y+T_{si}/2-W_D}{\alpha L_D}\right)\right) \quad (5.42)$$

The model correctly indicates that in tall fins V_{THF} is still governed by the lateral-gates whereas in thin fins the top-gate makes it decrease by coupling effect. Eq. (5.42) reduces to SG or DG cases for limit values of the geometry. For example, if $T_{si} < W_{Dmax}$ and $W_{fin} >> W_{Dmax}$, TG JL (symbols in Figure 5.27a) would act as SG JL (lines). Furthermore, for tall and narrow fins ($T_{si} >> W_{Dmax}$ and $W_{fin} < 2W_{Dmax}$), the behavior of the TG JL is similar to DG JL, as shown in Figure 5.27b.

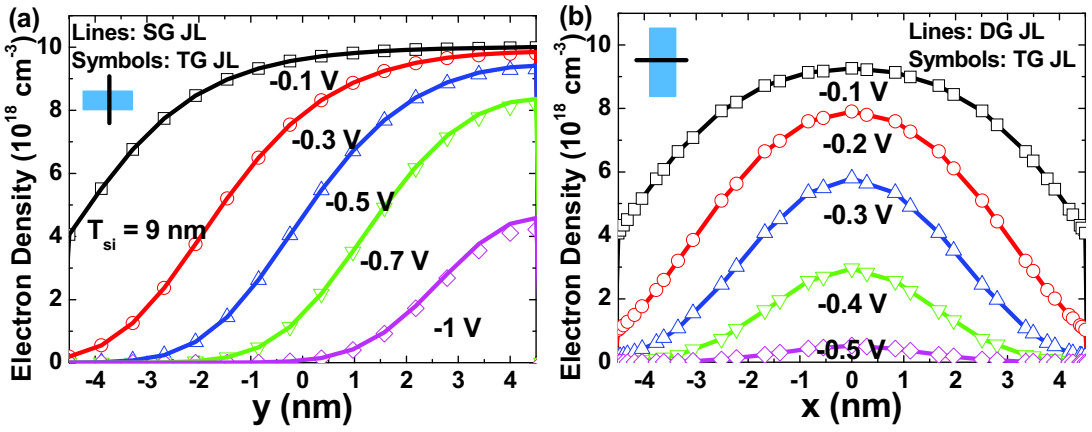

Figure 5.27: *(a) Comparison of simulated carrier profiles for SG and TG JL transistors (W_{fin} = 100 nm and T_{si} = 9 nm); (b) comparison of carrier profiles for DG and TG JL transistors (W_{fin} = 9 nm and T_{si} = 100 nm). L_G = 200 nm and $N_D = 10^{19}$ cm^{-3}. V_D = 0.05 V and V_{BG} = 0 V.*

For smaller geometry, the 3D coupling effect between the top and lateral-gates cannot be neglected. Figure 5.28 compares the simulated and modeled carrier density for a narrow and thin TG JL. Our model still matches well with the simulations for small V_{FG} (−0.1 V), close to the flat-band voltage (0 V). The subthreshold region is only qualitatively (not quantitatively) captured by our model.

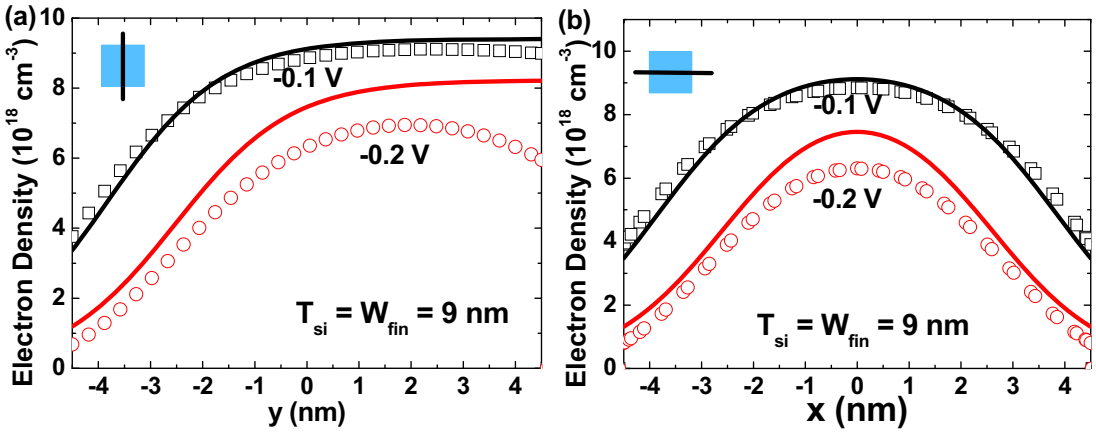

Figure 5.28: *Comparison of simulated and modeled carrier profiles in (a) vertical and (b) horizontal direction for nano Si TG JL with square cross-section. L_G = 200 nm and $N_D = 10^{19}$ cm^{-3}. V_D = 0.05 V and V_{BG} = 0 V. Solid lines: analytical model; open symbols: numerical simulations.*

2.3.2 Applications of carrier density model

Based on our empirical model of carrier profile in the channel, we can determine the threshold voltage. The integral of carrier profile in the channel yields the drain current. In addition, the maximum body size enabling full depletion can be estimated.

- **Extraction of threshold voltage from carrier profile**

Our extraction method for the threshold voltage is simply based on the defined criteria for the carrier density at G-point. These criteria, summarized in Table 5-IV, are determined from the analytical models of carrier profile for JL SOI FinFETs:

1) For SG JL, we have $T_{si} = W_D$ at V_{THF} and therefore the carrier density at G-point is: $N^*(T_{si}) = N_D/2$ calculated from Eq. (5.40).
2) For DG JL, we have $T_{si}/2 = W_D$ at V_{THF} and the carrier density at G-point is: $N^*(0) = N_D/4$ given by Eq. (5.41).
3) As shown in Figure 5.27, wide TG JL would act as SG JL and the behavior of the tall TG JL is similar to DG JL. Therefore, the criterion of SG JL can be used for wide TG JL and the criterion of DG JL can be used for tall TG JL. In very small TG JL, the location of point G is unknown, which prevents the use of Eq. (5.42).

Table 5-IV: *Threshold voltage definition based on the carrier density at G-point.*

SG JL	DG JL	Wide TG JL	Tall TG JL
$N^*(T_{si}) = N_D/2$	$N^*(0) = N_D/4$	$N^*(T_{si}) = N_D/2$	$N^*(0) = N_D/4$

The extracted threshold voltages are compared with the ones derived from the first peak of dg_m/dV_{FG}. The agreement between the two definitions of threshold voltage is remarkable (Figure 5.29) in SG and DG JL transistors for a very wide range of size and doping. Our method is straightforward and avoids second order derivatives and the effect of access resistance.

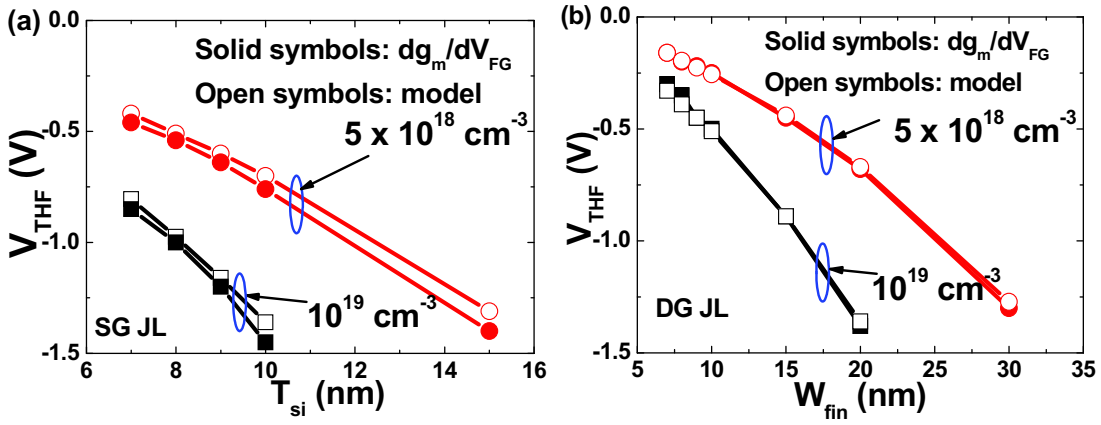

Figure 5.29: *Comparison of V_{THF} extracted with our method (open symbols) and dg_m/V_{FG} peak (solid symbols): (a) SG and (b) DG JL FETs.*

Our method can be easily adapted to wide or tall TG JL transistors, as shown in Figure 5.30. For thin TG JL (T_{si} = 9 nm), our method shows agreement with dg_m/dV_{FG} peak for relatively wide fin ($W_{fin} \geq 70$ nm for $N_D = 10^{19}$ cm^{-3} and $W_{fin} \geq 90$ nm for $N_D = 5 \times 10^{18}$ cm^{-3}). For narrow TG JL (W_{fin} = 9 nm), our method works for tall fins $W_{fin} \geq 40$ nm for $N_D = 10^{19}$ cm^{-3}. If the fin width or the film thickness shrinks, the deviation increases due to strong coupling effect between the three sides of the gate.

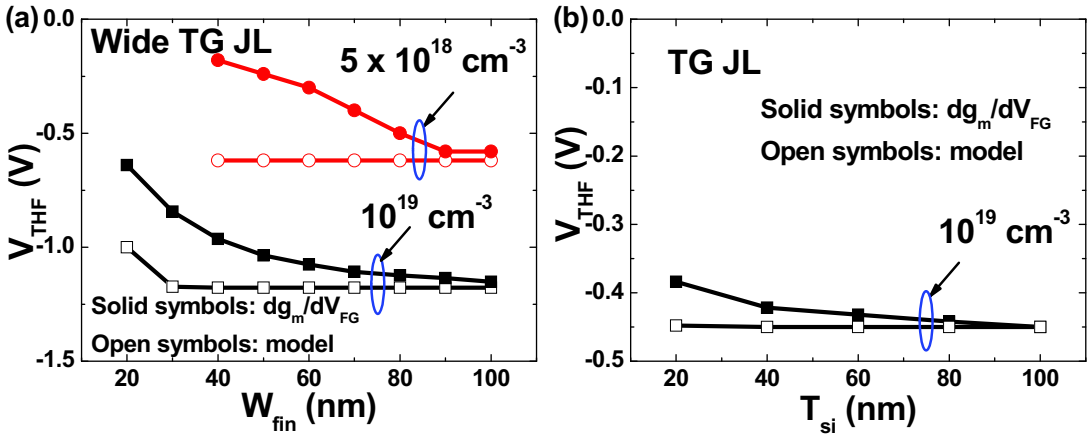

Figure 5.30: *Comparison of V_{THF} extracted with our method (open symbols) and dg_m/V_{FG} peak (solid symbols): (c) thin TG (T_{si} = 9 nm) and (d) narrow TG (W_{fin} = 9 nm) JL FinFETs.*

- **Drain current**

We assume that the volume mobility in partial depletion is a constant. The integral of carrier profile in the whole channel defines the drain current:

$$I_D = \begin{cases} \dfrac{W_{fin}}{L_G} \cdot q\mu_{vol} V_D \displaystyle\int_{-T_{si}/2}^{T_{si}/2} N^*(y)\,dy, & for\ SG\ JL \\ \dfrac{T_{si}}{L_G} \cdot q\mu_{vol} V_D \displaystyle\int_{-W_{fin}/2}^{W_{fin}/2} N^*(x)\,dx, & for\ DG\ JL \\ \dfrac{1}{L_G} \cdot q\mu_{vol} V_D \displaystyle\int_{-W_{fin}/2}^{W_{fin}/2} \int_{-T_{si}/2}^{T_{si}/2} N^*(x,y)\,dxdy, & for\ TG\ JL \end{cases} \tag{5.43}$$

where μ_{vol} is the volume mobility (108 cm^2/Vs for $N_D = 10^{19}$ cm^{-3} and 139 cm^2/Vs for $N_D = 5 \times 10^{18}$ cm^{-3}) [12]. These values of volume mobility are determined when both the front-and back-gates are biased at flat-band voltage. Figure 5.31 compares the simulated and modeled (Eq. (5.43)) drain current in both linear and semi-logarithmic scales for SG and DG JL devices. The results show that Eq. (5.43) works well in the partially-depleted region ($V_{FG} > V_{THF}$). Even for wide TG JL, the modeled drain

currents match well with the simulated ones in most of the partially-depleted region, except for the nonlinear deviation when V_{FG} is close to V_{THF} (Figure 5.32a). For narrow TG JL, the deviation increases as expected (Figure 5.32b).

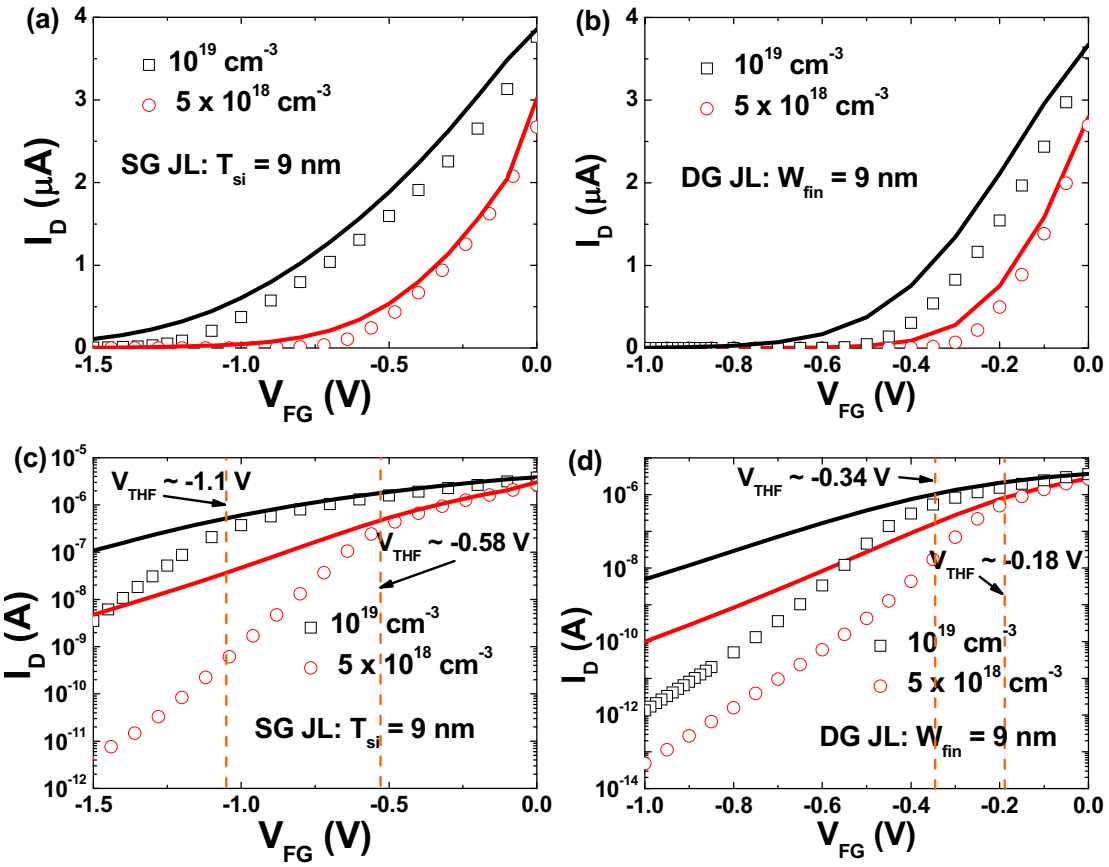

Figure 5.31: *Comparison of simulated and modeled (Eq. (5.43)) drain currents. (a) Linear and (c) semi-logarithmic scales for SG JL: W_{fin} = 100 nm and T_{si} = 9 nm. (b) Linear and (d) semi-logarithmic scales for DG JL: W_{fin} = 9 nm and T_{si} = 100 nm. L_G = 200 nm, V_D = 0.05 V and V_{BG} = 0 V. Open symbols: simulations; Solid lines: model.*

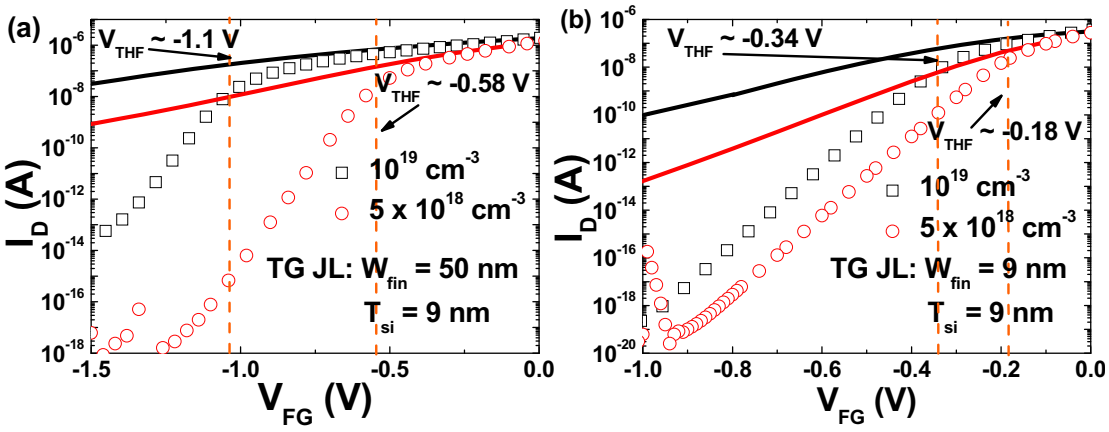

Figure 5.32: *Comparison of simulated and modeled (Eq. (5.43)) drain currents in triple-gate JL (Semi-logarithmic scale). (a) TG JL: W_{fin} = 50 nm and T_{si} = 9 nm and (b) TG JL: W_{fin} = 9 nm and T_{si} = 9 nm. L_G = 200 nm, V_D = 0.05 V and V_{BG} = 0 V. Open symbols: simulations; Solid lines: model.*

- **Evaluation of maximum body size**

Besides the determination of drain current and threshold voltage, the carrier profile is also very informative for optimizing the body thickness and doping. The maximum body thickness $T_{FD} = W_{Dmax}$ enabling the SG JL to turn-off is given by Eq. (2.16). For DG JL, the conventional definition for maximum body width is: $W_{FD} = 2W_{Dmax}$ (solid line in Figure 5.33). The dotted line shows that the maximum W_{fin} enabling the JL FET to switch off is actually larger. The inter-gate coupling effect, included in our model, indicates a more efficient body depletion, resulting from the cooperation of the two gates and allows for an increase of W_{fin} that is beneficial in terms of drive current.

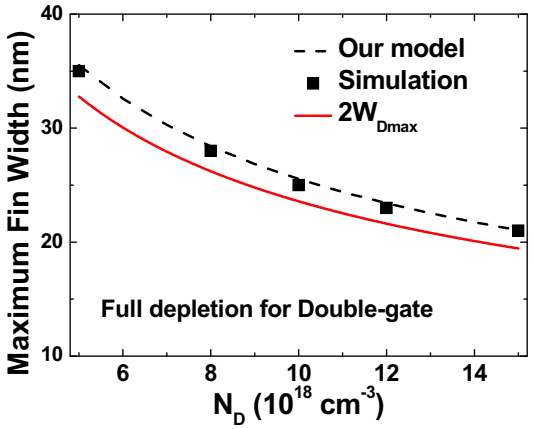

Figure 5.33: *Maximum body size to achieve switch-off in DG JL FET.*

The maximum carrier density for DG JL is reached at x = 0 and can be calculated from Eq. (5.41):

$$N^*(0) = \frac{N_D}{4}\left(1 + tan\,h\left(\frac{W_{fin}/2 - W_D}{\alpha L_D}\right)\right)^2 \tag{5.44}$$

Eq. (5.44) describes the dependence of the maximum carrier concentration at G-point on fin width. Reciprocally, if N_{FD} is defined as the carrier concentration needed to achieve full depletion, we can determine from Eq. (5.44) the maximum fin width W_{FD} for DG JL:

$$W_{FD} = 2W_{Dmax} - \alpha L_D\, ln\left(\sqrt{\frac{N_D}{N_{FD}}} - 1\right) \tag{5.45}$$

Since the carrier density at G-point for SG JL is equal to $N_D/2$ for $V_G = V_{THF}$, the W_{FD} value for DG JL is calculated from Eq. (5.45) with $N_{FD} = N_D/2$. In order to validate Eq. (5.45), we compare the calculated (dashed line in Figure 5.33) and simulated (symbols in Figure 5.33) maximum body size. The simulated maximum body size is determined when the carrier density at G-point is equal to $N_D/2$. The two curves coincide well and confirm that the conventional approximation ($2W_{Dmax}$) is underestimating the body size (solid line in Figure 5.33).

In summary, we have presented a model for 1D, 2D and 3D carrier profiles in the body of JL transistors. The model is compact and very attractive because it avoids the solving of Poisson equation and the modeling of the potential. Although it may look simplistic of naive, our carrier profile model can provides the threshold voltage, the drain current and the maximum body size enabling the full depletion. In all models, the doping concentration of the channel and the carrier mobility need to be known. In the following, we will investigate methods to extract the flat-band voltage, doping concentration and low-field mobility of the channel in the accumulation region.

2.4 Parameters extraction in accumulation mode

Until now we have focused on the full and partial depletion regimes. For pragmatic applications, the knowledge of flat-band voltage, mobility and doping concentrations is critical. In order to access these parameters, we need to focus on the accumulation regime. Meanwhile, we will revisit the conventional extraction methods and show their limits in the nano-channel JL SOI FinFETs.

2.4.1 Extraction of flat-band voltage

The conventional method to determine the flat-band voltage is based on dg_m/dV_{FG}. As previously demonstrated in section 2.2.3, this method does not work in nano-channel JL SOI FinFETs. According to [25], [28], in accumulation mode, the drain current for a JL transistor is the sum of volume (I_{vol}) and accumulation (I_{acc}) currents. In wide TG JL, we assume that the volume current does not vary with V_{FG} [30]. For the accumulation part, we independently consider the two lateral-gates and the top-gate. Therefore, the drain current can be modeled as:

$$\begin{aligned} I_D(TG) &= I_{vol} + I_{acc} \\ &= \frac{W_{fin} \times T_{si}}{L_G} \cdot qN_D\mu_{vol}V_D + \frac{W_{fin} + 2T_{si}}{L_G} \cdot \mu_{acc}C_{ox}\left(V_{FG} - V_{FBF}\right)V_D \end{aligned} \tag{5.46}$$

This equation implies a negligible coupling between gates in accumulation mode. For "weak" accumulation, this hypothesis is fully acceptable. Therefore, the drain current is proportional to W_{fin}, as shown in Figure 5.34a. Letting $W_{fin} \to 0$, we can obtain the accumulation current induced by the lateral-gates from the intercept with the vertical axis (positive current in Figure 5.34b). However, Eq. (5.46) only works for $V_{FG} > V_{FBF}$. When we trace the intercept current versus front-gate voltage for $V_{FG} < V_{FBF}$ (in partial depletion mode, the current flowing into the channel is only the volume current of the partially-depleted film, we obtain a negative value in Figure 5.34b. This change of sign for the intercept current is a good way to identify V_{FBF}.

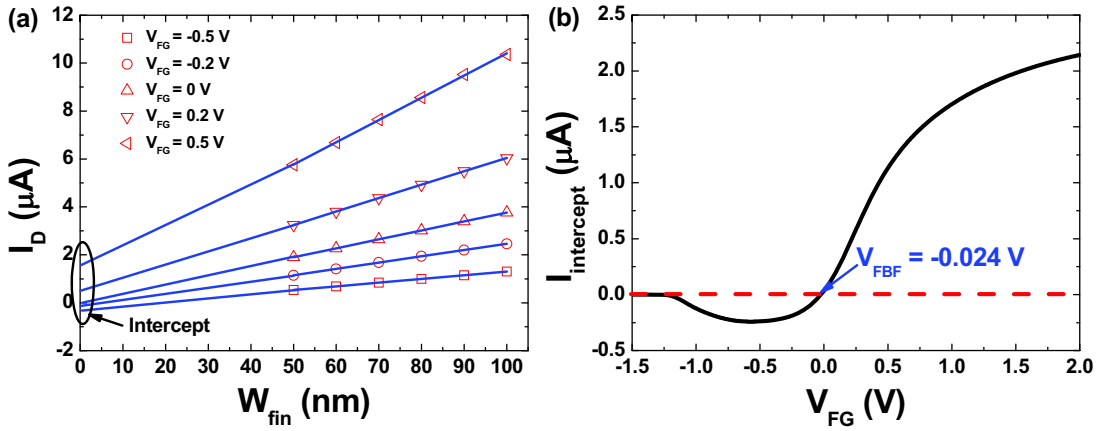

***Figure 5.34**: (a) I_D versus W_{fin} and (b) the intercept current versus V_{FG}. W_{fin} = 50 ~ 100 nm.*

We compare the intercept current obtained from wide (solid line in Figure 5.35a) and narrow (dashed line in Figure 5.35a) JL SOI FinFETs. The intercepts with the vertical axis are different. Therefore, the linear relationship between I_D and W_{fin} disappears in narrower JL SOI FinFETs due to enhanced coupling effect. However, no matter how small W_{fin} is, the intercept current will intersect with the zero current line for $W_{fin} \to 0$ and $V_{FG} = V_{FBF}$ (no current flow in the channel). Figure 5.35b shows that the intercept currents obtained from different combinations of fin width (100 & 50 nm; 50 & 20 nm, 20 & 10 nm, 10 & 9 nm and 9 & 7 nm). The sign of all the intercept currents changes at the same point, which corresponds to the flat-band voltage.

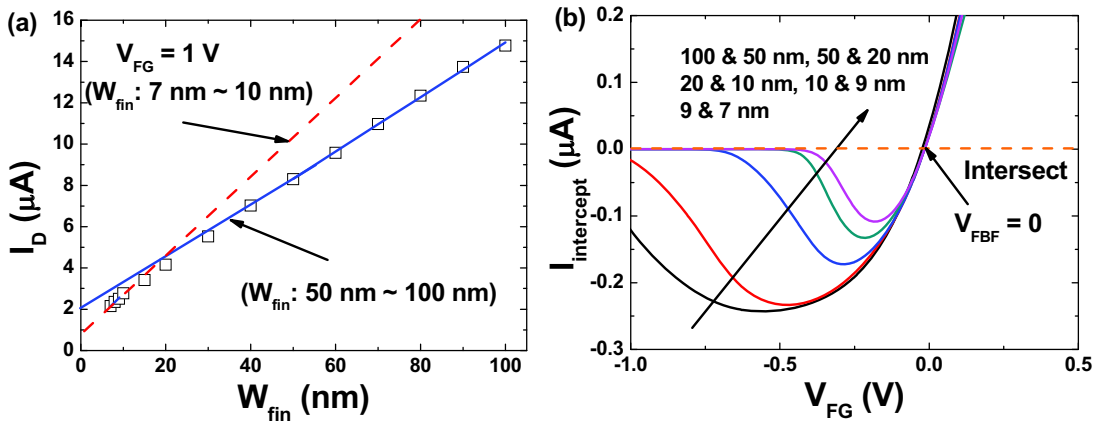

Figure 5.35: *(a) Comparison of I_D for different fin width and (b) the intercept current versus V_{FG} for arbitrary couples of JL SOI FinFETs.*

The theoretical V_{FBF} is calculated as the difference of work-functions between the front-gate and the channel. Table 5-V gives the V_{FBF} extracted with our method, which is equal to the theoretical V_{FBF}. In order to further verify this method, we changed the work-function of the front-gate. The extracted V_{FBF} still shows good agreement with theoretical V_{FBF}. Next, we will describe how to use the Y-function Y_{acc} defined in Eq. (2.21) of chapter 2 to extract the V_{FBF} and low-field mobility.

Table 5-V: *Extracted V_{FBF} for narrow JL SOI FinFETs with different front-gate work-function.*

Work-function (V)		**Theoretical V_{FBF} (V)**	**Extracted V_{FBF} (V)**		
Front-gate	Channel		dg_m/dV_{FG}	$I_{intercept}$	Y_{acc}
4.08	4.08	0	0.004	0	0
4.32	4.08	0.24	0.26	0.23	0.24
4.9	4.08	0.82	0.85	0.81	0.82

2.4.2 Extraction of mobility

Based on current-voltage measurements, several methods of mobility extraction have been conceived earlier for junctionless transistors [19], [25], [29], [30]: $1/g_m^2$ and the modified Y-function $(dY/dV_{FG})^2$. We will revisit them, show their limits in nano-channel JL SOI FinFETs, and then propose our new methods.

- **Conventional methods to extract volume mobility: $1/g_m^2$**

For a planar JL transistor, the drain current in partial depletion region is expressed as:

$$I_D = \frac{W_{fin}}{L_G}\left(T_{si} - W_D\right) qN_D \mu_{vol} V_D \tag{5.47}$$

where W_D is the width of depletion region (Eq. (5.39) with $V^* = 0$). Jeon *et al.* proposed using $1/g_m^2$ to extract flat-band voltage (V_{FBF}) and volume mobility (μ_{vol}) for planar JL transistors [29]:

$$\frac{1}{g_m^{\,2}} = \frac{1}{\left(\frac{W}{L_G}\cdot\mu_{vol}\cdot V_D\cdot C_{OX}\right)^2} - \frac{2}{\left(\frac{W}{L_G}\cdot\mu_{vol}\cdot V_D\right)^2\cdot q\cdot\varepsilon_{si}\cdot N_D}\left(V_{FG} - V_{FBF}\right) \tag{5.48}$$

Once the doping concentration of the channel is known [25], μ_{vol} can be extracted from the slope of $1/g_m^2(V_{FG})$. Using the extracted μ_{vol}, we can calculate the flat-band voltage V_{FBF} from the intercept of $1/g_m^2(V_{FG})$ with the vertical axis (V_{FG} = 0 V). For wide JL SOI FinFETs ($W_{fin} \gg T_{si}$), the channel is mainly depleted by top-gate and the depletion triggered by lateral-gates can be neglected. Therefore Eq. (5.48) still works in wide JL SOI FinFET, as shown in Figure 5.36a. The extracted low-field mobility and flat-band voltage are respectively 108 cm^2/Vs and 0.05 V. Both of them are close to the input values (110 cm^2/Vs for volume mobility and 0 V for flat-band voltage). However, in narrow fin (Figure 5.36b), $1/g_m^2$ is not linear in partial depletion region due to the increasing importance of depletion regions triggered by lateral-gates.

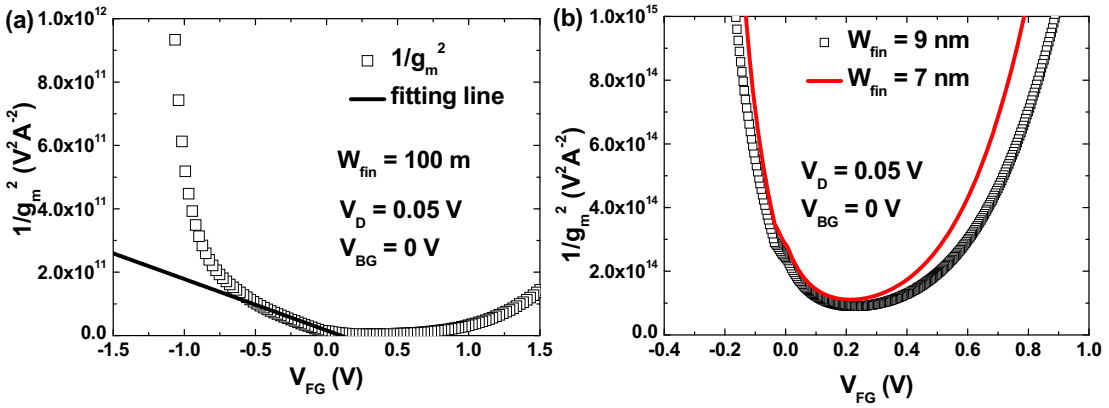

Figure 5.36: *Simulated $1/g_m^2$ versus V_{FG} for wide and narrow JL SOI FinFETs. (a) W_{fin} = 100 nm and (b) W_{fin} = 9 & 7 nm. T_{si} = 9 nm, L_G = 200 nm and $N_D = 10^{19}$ cm^{-3}.*

- **Conventional methods to extract low-field mobility: $(dY/dV_{FG})^2$**

In [25] and [31], the modified Y-function $(dY/dV_{FG})^2$ was used to determine the low-field mobility in planar junctionless transistors. It is assumed that the accumulation and volume currents can be separated and the volume current is independent of V_{FG} in accumulation regime. This assumption corresponds to our earlier demonstration in heavily-doped film [28]. Therefore, we can write $(dY/dV_{FG})^2$ as:

$$\left(\frac{dY}{dV_{FG}}\right)^2 = \frac{W}{L_G}\cdot C_{OX}\cdot \mu_0 \cdot V_D \tag{5.49}$$

The low-field mobility can be determined from $(dY/dV_{FG})^2$ at a fixed V_{FG}, as shown in Figure 5.37a. Here, we extracted low-field mobility at V_{FG} = 0.2 V to avoid strong coupling effect. The extracted low-filed mobility in planar junctionless transistors is ~ 110 cm^2/ Vs, equal to the volume mobility. We will show that the volume current can increase with V_{FG} in accumulation regime of JL SOI FinFETs, which will be introduced in our method of mobility extraction. Therefore, $(dY/dV_{FG})^2$ does not have the flat region in the accumulation regime, as shown in JL SOI FinFET (Figure 5.37b).

In general, the conventional extraction methods for both volume and low-field mobility do not work in the nano-channel JL SOI FinFETs due to the coupling effect; next we will introduce our methods to determine the low-field mobility.

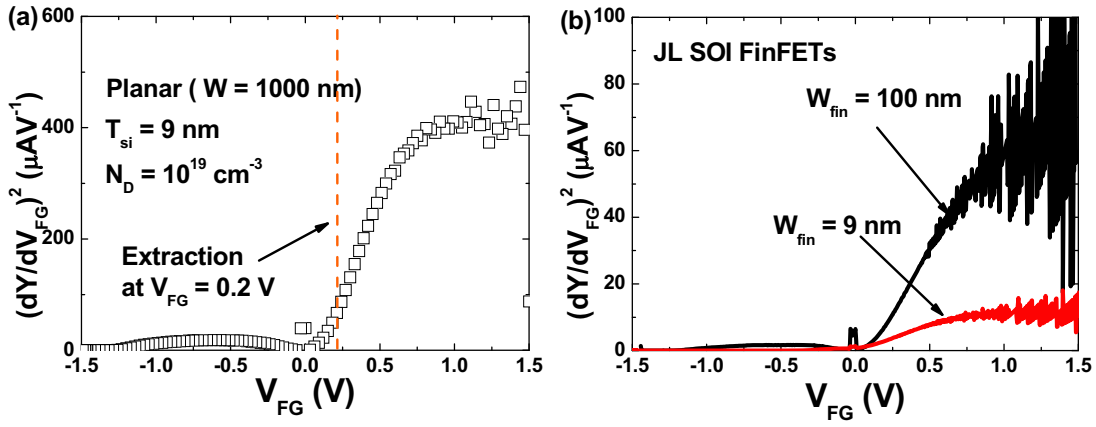

Figure 5.37: *$(dY/dV_{FG})^2$ for: (a) long planar JL transistor and (b) JL SOI FinFETs.*

- **A new method to extract low-field mobility in weak accumulation**

When JL SOI FinFETs work in the accumulation mode, the majority carriers will accumulate in the film near the gate oxide, as shown in Figure 5.38a. Therefore, the minimum of electron density in the channel reflects the volume conduction. In the JL SOI FinFETs (especially narrow fin), the electron density in the volume increases with the front-voltage due to the strong coupling effect from lateral-gates. Figure 5.38b shows the enhancement of minimum of electron density with the front-gate voltage. In order to identify a weak-coupling region, where 1D model can still work, we define a criterion for the minimum of electron density in the channel. If the variation of the electron density is smaller than 15%, we assume that the coupling effect in that region can be neglected. From Figure 5.38b, we find the coupling effect can be neglected when V_{FG}–V_{FBF} < 0.2 V for this nano-channel JL with W_{fin} = 9 nm and T_{si} = 9 nm. When the silicon thickness increases to 100 nm, the weak coupling effect region enlarges (V_{FG}–V_{FBF} < 0.4 V), as shown in Figure 5.39. This can be attributed to the decrease of the effect of top-gate.

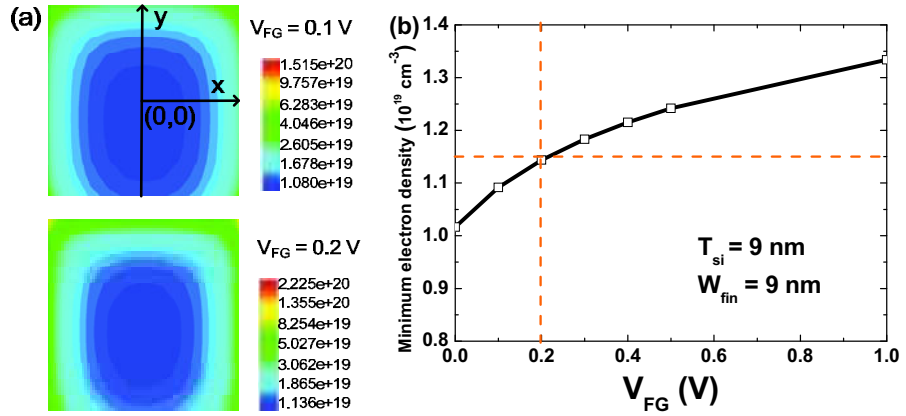

***Figure 5.38**: (a) Electron densities contours in the middle of the channel for a nano-channel JL SOI FinFET (W_{fin} = 9 nm and T_{si} = 9 nm) with V_{FG} = 0.1 V and V_{FG} = 0.2 V and (b) minimum electron densities along x = 0 for different V_{FG}.*

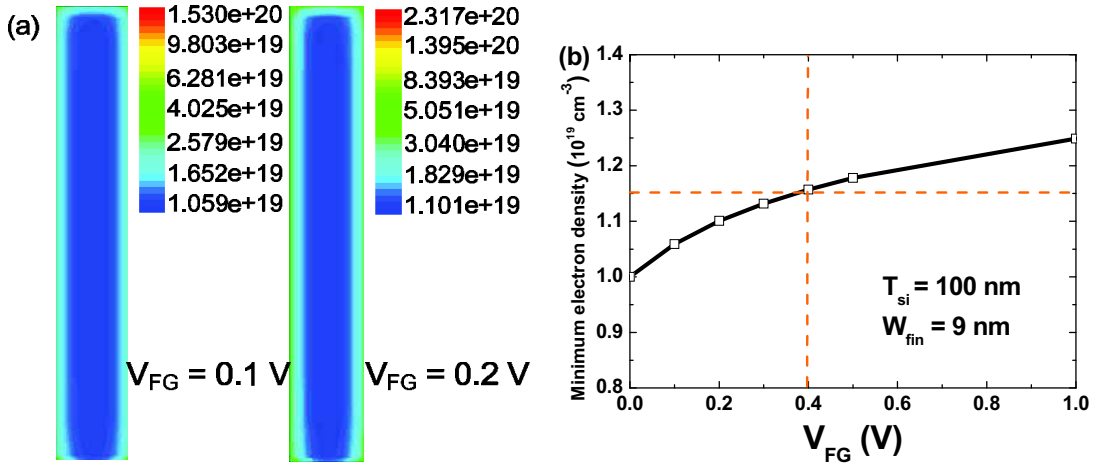

***Figure 5.39:** (a) Electron densities contours in the middle of the channel for a narrow and tall JL SOI FinFET (W_{fin} = 9 nm and T_{si} = 100 nm) with V_{FG} = 0.1 V and V_{FG} = 0.2 V and (b) minimum electron densities along x = 0 for different V_{FG}.*

In order to demonstrate that coupling effect can be neglected if the minimum of electron density varies less than 15%, we compare the $I_D(V_{FG})$ curves between SG, DG and TG JL SOI FinFETs. We assume that the 1D current model still works [33]. The accumulation current for TG JL can be expressed as:

$$I_{acc}(TG) = I_D(TG) - I_{vol} = \frac{W_{fin} + 2T_{si}}{L_G} C_{OX} \mu_{acc} V_D \cdot (V_{FG} - V_{FBF}) \qquad (5.50)$$

Here, I_{vol} denotes the volume current. Similarly, the accumulation current for DG JL can be written as:

$$I_{acc}(DG) = I_D(DG) - I_{vol} = \frac{2T_{si}}{L_G} C_{OX} \mu_{acc} V_D \cdot (V_{FG} - V_{FBF}) \tag{5.51}$$

Combing Eq. (5.50) with Eq. (5.51), we have:

$$\frac{I_{acc}(TG)}{I_{acc}(DG)} = \frac{W_{fin} + 2T_{si}}{2T_{si}} \tag{5.52}$$

If the volume current does not vary with V_{FG}, the difference of I_D between triple- and lateral-gates mainly results from the different geometric factor of accumulation current. Figure 5.40a compares the drain current between DG and TG JL with different film thickness. It is clear that the drain current for TG is larger than that for DG JL. With the film thickness shrinking, this difference of drain current enhances. Figure 5.40b compares $I_{acc}(TG)/I_{acc}(DG)$ with $(W_{fin}+2T_{si})/2T_{si}$ under low and high front-gate bias. Here, I_{vol} equals to the I_D (TG) for $V_{FG} = V_{FBF}$. Under low front-gate bias (V_{FG}–V_{FBF} < 0.5 V), $I_{acc}(TG)/I_{acc}(DG)$ almost equals to $(W_{fin}+2T_{si})/2T_{si}$ for all kinds of film thickness; under high front-gate bias (V_{FG}–V_{FBF} > 0.5 V), $I_{acc}(TG)/I_{acc}(DG)$ approaches $(W_{fin}+2T_{si})/2T_{si}$ only for wider devices (W_{fin} > 60 nm).

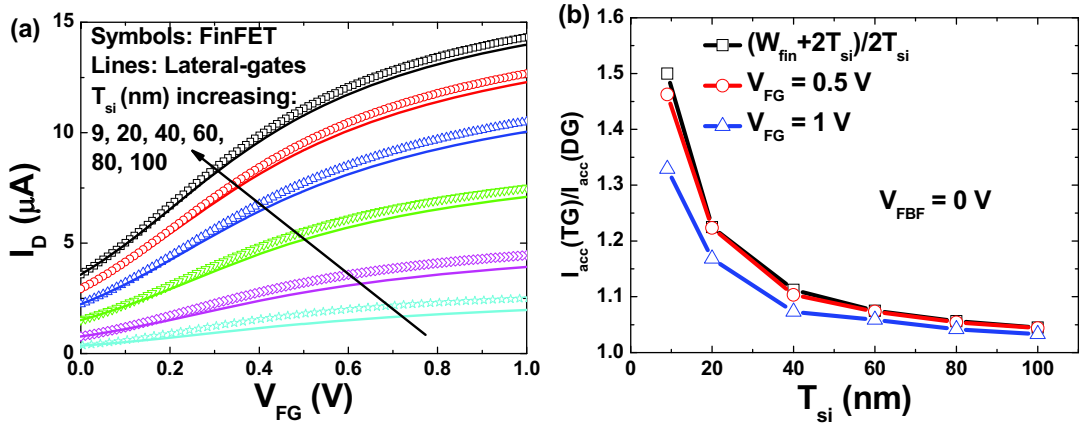

Figure 5.40: *(a) Comparison of drain current between TG and DG with different film thickness and (b) $I_{acc}(TG)/I_{acc}(DG)$ versus film thickness under low and high front-gate bias. W_{fin} = 100 nm.*

We now compare the currents between SG and TG JL. The 1D model for accumulation current of SG JL is expressed as:

$$I_{acc}(SG) = I_D(SG) - I_{vol} = \frac{W_{fin}}{L_G} C_{OX} \mu_{acc} V_D \cdot (V_{FG} - V_{FBF}) \tag{5.53}$$

Dividing Eq. (5.50) by Eq. (5.53), we have:

$$\frac{I_{acc}(TG)}{I_{acc}(SG)} = \frac{W_{fin} + 2T_{si}}{W_{fin}} \tag{5.54}$$

The drain current of SG differs remarkably from that of TG (Figure 5.41a). Only under very low front-gate bias (V_{FG}–V_{FBF} < 0.2 V), $I_{acc}(TG)/I_{acc}(SG)$ coincides with $(W_{fin}+2T_{si})/W_{fin}$ for all fin widths (Figure 5.41b); under high front-gate bias (V_{FG}–V_{FBF} > 0.2 V), $I_{acc}(TG)/I_{acc}(SG)$ equals $(W_{fin}+2T_{si})/2T_{si}$ for wider devices (W_{fin} > 60 nm), as shown in Figure 5.41c. The deviation increases with fin width shrinking.

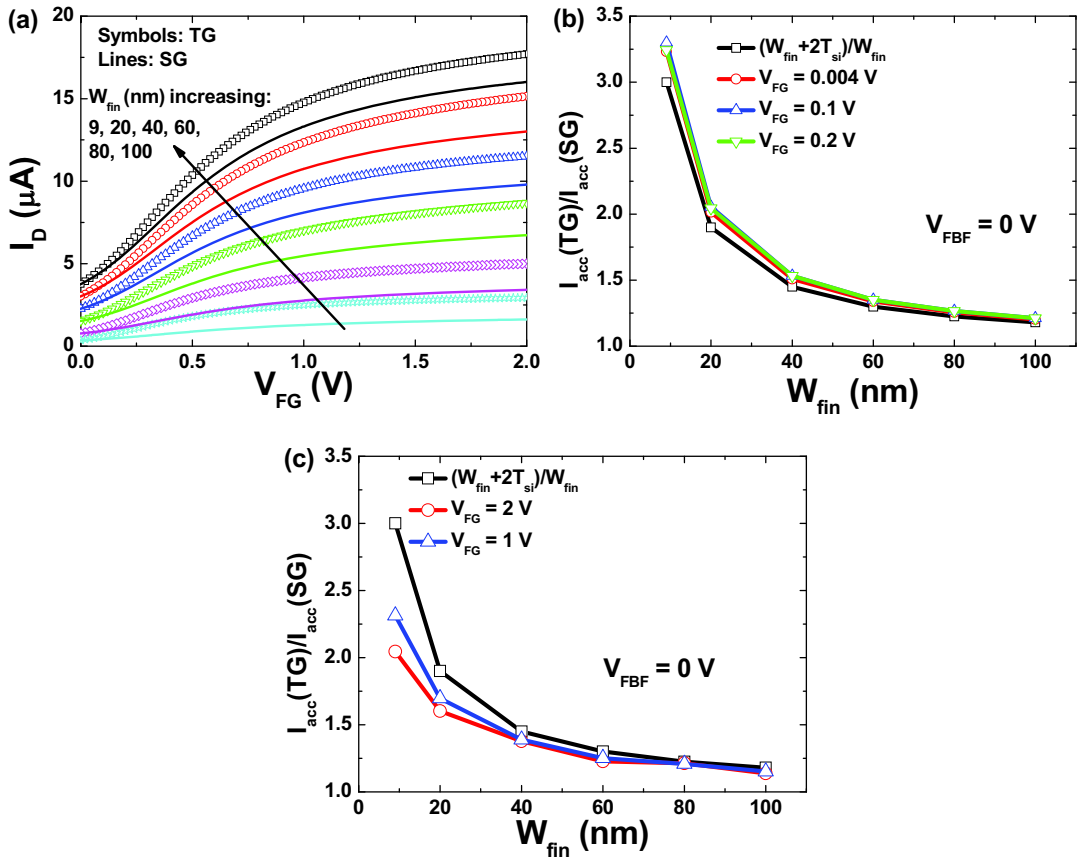

Figure 5.41: *(a) Comparison of drain current between SG and TG JL devices with different fin width; $I_{acc}(TG)/I_{acc}(SG)$ versus fin width under (b) low and (c) high front-gate bias. T_{si} = 100 nm*

Combining the comparisons of drain currents among the three structures (SG, DG and TG), we determine the region where the coupling effect can be neglected: V_{FG}–V_{FBF} < 0.2 V. Consequently, applying the conventional Y-function to accumulation current in TG JL (Eq. (5.50)), we have:

$$Y_{acc}(TG) = \frac{I_{acc}(TG)}{\sqrt{g_m}} = \left(\frac{W_{fin} + 2T_{si}}{L_G} \cdot C_{OX} \cdot \mu_0 \cdot V_D \right)^{1/2} (V_{FG} - V_{FBF}) \qquad (5.55)$$

The intercept of Eq. (5.55) accurately determines the flat-band voltage and the low-field mobility can be calculated from the slope, as shown in Figure 5.42. The extracted low-field mobility is very close to the volume mobility (110 $cm^2/(V \cdot s)$) [12]. This can be explained by the negligible effect of front-gate bias on the mobility in "weak" accumulation region ($\mu_{vol} \approx \mu_0$). The extracted flat-band voltages are fully equal to the theoretical values (Table 5-V).

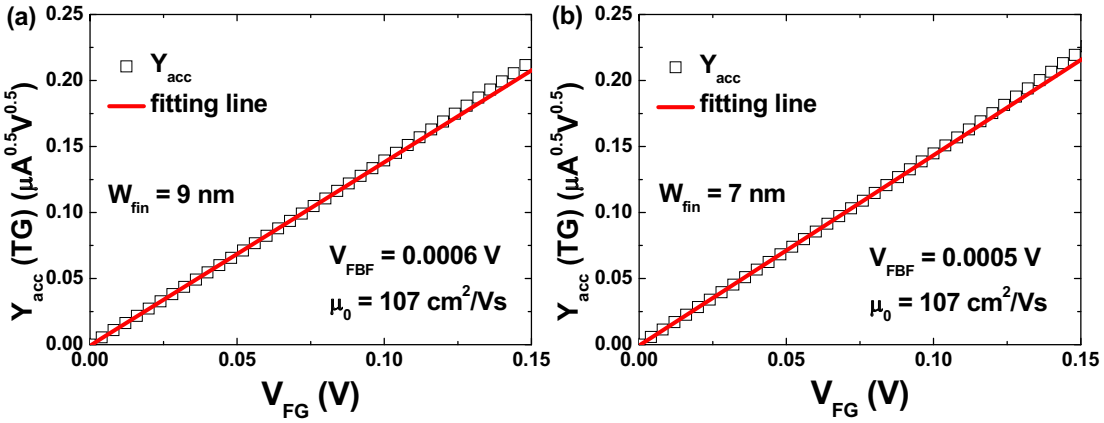

Figure 5.42: *Application of Y_{acc} (Y-function method) to the narrow TG JL. (a) W_{fin} = 9 nm and (b) W_{fin} = 7 nm.*

2.4.3 Extraction of doping concentration

For $V_{FG} = V_{FBF}$, there is volume conduction. Therefore, the doping concentration of the channel can be calculated as:

$$N_D = \frac{L_G I_D(TG)}{W_{fin} T_{si} q \mu_{vol} V_D} \quad for \quad V_{FG} = V_{FBF} \qquad (5.56)$$

In the region of "weak" accumulation (V_{FG}–V_{FBF} < 0.2 V), where coupling effect can be neglected, the surface scattering is modest and the low-field mobility is close to the volume mobility ($\mu_{vol} \approx \mu_0$). Substituting the low-field mobility extracted from Eq.(5.55) into Eq. (5.56), the doping level can be calculated. For W_{fin} = 9 nm and W_{fin} = 7 nm, the extracted doping concentrations are: 1.08 × 10^{19} cm^{-3} and 1.1 × 10^{19} cm^{-3}, respectively. They are close to the input value (10^{19} cm^{-3}).

2.5 Conclusions on modeling of JL SOI FinFETs for parameters extraction

We have modeled the potential distribution in full depletion region and the carrier profile in the partially-depleted region. Based on these two models, we have developed methods to define and extract the threshold voltage in nano-channel JL SOI FinFETs. However, these methods need the flat-band voltage and doping concentration of the channel. This is why we have also proposed simple methods to extract flat-band voltage, mobility and doping concentration of the channel in the "weak" accumulation region. The pragmatic extraction flow is shown in Figure 5.43 and described as follows:

1) The starting point is the extraction of flat-band voltage (V_{FBF}) from $I_{intercept}$ described in section 2.4.1.
2) With the flat-band voltage (V_{FBF}), we can obtain the low-field mobility (μ_0) from Y_{acc} in Eq. (5.55) in the "weak" accumulation region.
3) Since the low-field mobility in the "weak" accumulation region is close to the volume mobility ($\mu_0 \approx \mu_{vol}$), we can calculate the doping concentration of the channel (N_D) from the drain current at $V_{FG} = V_{FBF}$ (Eq. (5.56)).
4) With the flat-band voltage and the doping concentration of the channel, we can extract the threshold voltage from:
   - 2D potential model in full depletion region in Eq. (5.34);
   - carrier profile model in partial depletion region described in section 2.3.2.

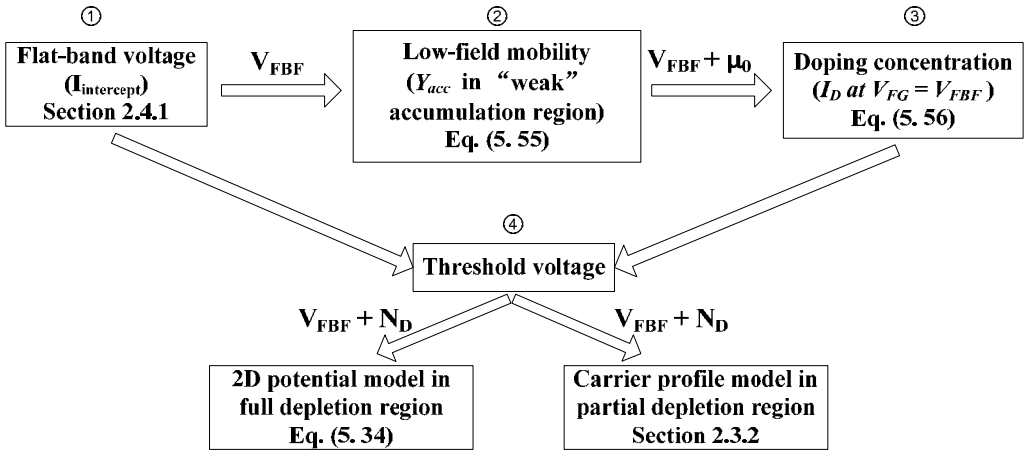

Figure 5.43: *Parameters extraction flow for JL SOI FinFETs.*

All the results shown in Part B are so far confirmed by simulations. In Part C, we will apply these methods to experimental data on GaN junctionless FinFETs.

Part C: Application for parameters extraction in experimental GaN junctionless FinFETs

2.6 Experimental results

Although the proposed models have been developed and simulated for silicon, they can be easily adapted to other metal-insulator-semiconductor structures. K-S. Im *et al.* proposed a heterojunction-free GaN JL FinFET [34], as shown in Figure 5.44. The width and height of the fin are respectively 60 nm and 120 nm. A 20 nm Al_2O_3 layer was deposited on the Si-doped GaN as gate insulator. The doping concentration of the channel is around 10^{18} cm^{-3}, measured by Hall effect experiment before the devices were fabricated.

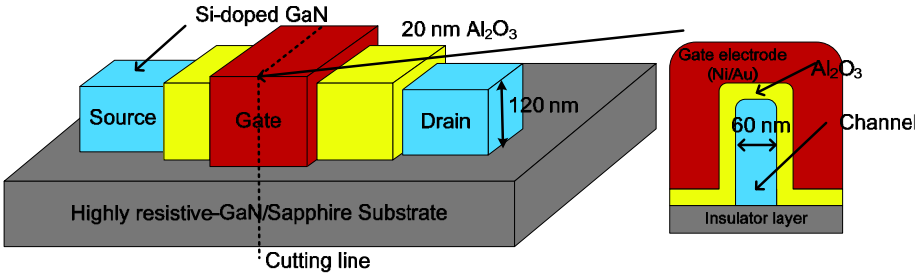

Figure 5.44: *Schematic structure and cross-section of a GaN nano-channel JL FinFET.*

A steep switching characteristic is observed in $I_D(V_{FG})$ curve (Figure 5.45a). Two peaks appear in the $g_m(V_{FG})$ curve (Figure 5.45b). This reveals three operating modes, similar to JL SOI transistors (see Figure 5.10a). Therefore, the extraction method for JL SOI FinFET can be used for GaN FinFET. Two peaks are observed in the $dg_m/dV_{FG}(V_{FG})$ curve of the GaN FinFETs (Figure 5.46a). This first peak defines V_{FBF}.

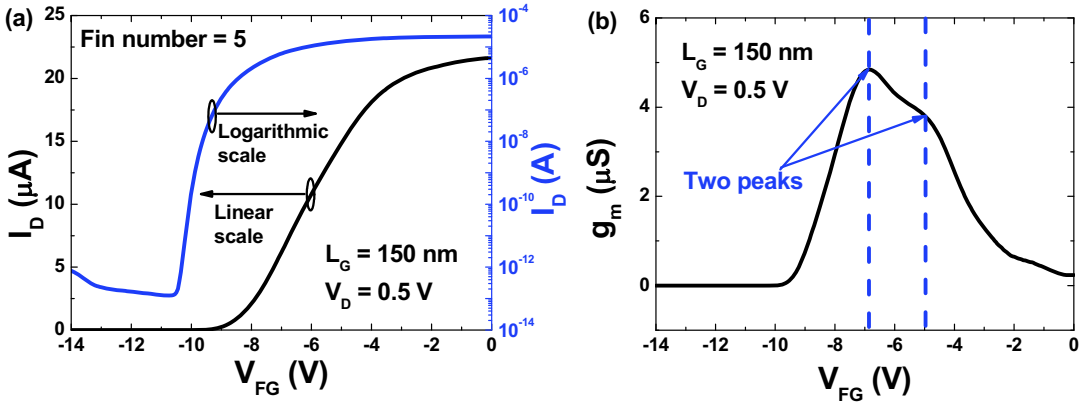

Figure 5.45: *Typical curves for a five-finger GaN JL FinFET: (a) I_D versus V_{FG} and (b) g_m versus V_{FG} (L_G = 150 nm). The number of fin is equal to 5.*

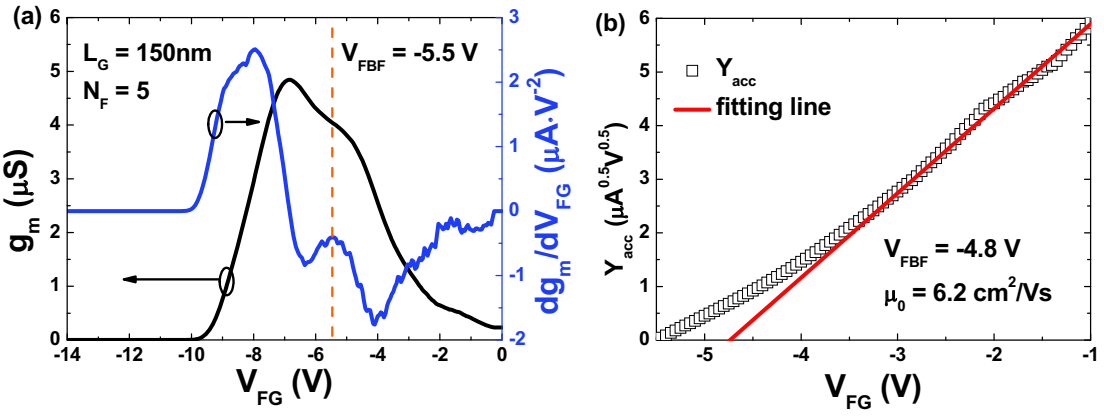

Figure 5.46: *(a) dg_m/dV_{FG} versus V_{FG} and (b) adapted Y-function Y_{acc} versus V_{FG} for a five-finger GaN JL FinFET (L_G = 150 nm).*

For a 20 nm Al_2O_3 layer, the maximum depletion width of GaN with doping concentration 10^{18} cm^{-3} is ~ 37 nm (calculated from Eq. (2.17)). This demonstrates that the lateral-gates play a main role in the depletion of the 60 nm wide channel. All the extracted parameters are summarized in Table 5-VI.

1) **The flat-band voltage** (−4.8 V) is only extracted from Eq. (5.55), as shown in Figure 5.46b. It is close to the value (−5.5 V) determined from the peak of dg_m/dV_{FG} (Figure 5.46a). Note that the volume current used for the determination of accumulation current in Eq. (5.50) is the drain current when the front-gate voltage is equal to the flat-band voltage extracted from dg_m/dV_{FG}.
2) **The low-field mobility** is 6.2 cm^2/Vs, extracted from Eq. (5.55). It is far smaller than the one measured from Hall effect (234 cm^2/Vs) [34]. This may be explained by the mobility degradation due to high traps densities at Al_2O_3/GaN interface generated during fabrication.
3) **The doping concentration of the channel** is extracted from Eq. (5.56). The volume current used is the drain current for $V_{FG} = V_{FBF} = -5.5$ V. The volume mobility is replaced by the low-field mobility (6.2 cm^2/Vs). The extracted doping concentration is 10^{18} cm^{-3}, which is equal to the one measured from Hall effect.
4) **The threshold voltage** is determined by two methods:
   — The first one is based on the 2D potential model in the subthreshold region. Substituting this extracted doping concentration (10^{18} cm^{-3}) and flat-band voltage (−5.5 V) in Eq. (5.34), we obtain the threshold voltage (−7.3 V). It is

close to the sharp decrease point of the drain current in the semi-logarithmic scale (Figure 5.45a).

— The second one is based on the model of carrier profile in partial depletion region. Since the film thickness of GaN FinFET (120 nm) is twice larger than its fin width (60 nm), we regard it as tall DG JL transistors. Thus, the criterion of carrier density at G-point for GaN FinFET is 0.25×10^{18} cm^{-3}. Here, we use $V^* = 0$ and $V_{FBF} = -5.5$ V in Eq. (5.39). The extracted threshold voltage is −7.8 V, a little smaller than the one (−7.3 V) extracted from Eq. (5.34). This can be explained by the shape of the GaN FinFET, which is neither DG nor tall TG.

Table 5-VI: *Comparison of extracted parameters from our methods and other methods.*

V_{FBF} (V)		μ_0 (cm^2/Vs)		N_D (10^{18} cm^{-3})		V_{THF} (V)	
dg_m/dV_{FG}	Our method	Hall effect	Our method	Hall effect	Our method	Potential model	Model of carrier profile
−5.5	−4.8	234	6.2	1	1	−7.3	-7.8

3. Conclusions and perspectives

In this chapter, the 3D coupling effect between the lateral-gates and the back-gate was measured in inversion-mode vertical double-gate SOI FinFETs. We proposed a 2D analytical model to determine the 2D potential profile within the body and explain the coupling effects. The very good agreement obtained between experimental and modeling results validate the model. Thanks to the thick insulating layer at the top of the fin in vertical DG FinFET, the action of the vertical electric field from top to bottom is relaxed and the back-gate effect is enhanced. Therefore, vertical DG FinFETs are more sensitive to back-gate biasing than triple-gate FinFETs. The difference between these two transistor structures tends to vanish in ultra-narrow fins. DG FinFETs with moderate fin width are suitable devices for dynamic threshold voltage control using thin BOX, ground plane and back biasing schemes [35], [36]. The coupling effect improves the performance of device in particular for multiple threshold voltage application [37].

This 3D coupling effect has been extended to JL SOI FinFETs. Firstly, we adapted the 2D potential model of inversion-mode SOI FinFETs to junctionless SOI FinFETs. It works well in the full depletion region. For the partial depletion region, we developed a compact model of carrier profile in single-, double- and triple-gate JL SOI FinFETs. Despite its simplicity, this analytical model yields surprising accurate results. In the accumulation region, the conventional 1D model cannot be applied directly due to the strong coupling effect in the nano-channel JL SOI FinFETs. 3D TCAD simulations show that this coupling effect can be neglected in the "weak" accumulation region. Table 5-VII summarizes how to use these models to extract parameters in JL SOI FinFETs.

The parameters extraction methods have been tested on experimental results for heavily-doped GaN FinFETs. The extracted doping concentration shows agreement with Hall effect measurements. The proposed models can be used for analysis of the coupling effect, characterization and optimization of geometry in any other heavily-doped FinFETs.

Table 5-VII: *Summary of proposed models for parameters extraction in JL SOI FinFETs.*

Mode	Model	Input parameters	Extracted parameters
Full depletion	Eq. (5.34)	V_{FBB} and N_D	V_{THF}
Partial depletion	Section 2.3.2	V_{FBB} and N_D	V_{THF}
	Eq. (5.43)	V_{FBB}, N_D and μ_{vol}	I_D
	Eq. (5.45)	V_{FBB}, N_D and N_{FD}	W_{FD}
"Weak" accumulation	Section 2.4.1	At least two W_{fin}	V_{FBB}
	Eq. (5.55)	V_{FBB} and I_D	$\mu_0 \approx \mu_{vol}$
	Eq. (5.56)	V_{FBB}, I_D *and* μ_{vol}	N_D

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Chapter 6: General conclusions and perspectives

During this PhD, I focused on the electrical characterization and transport modeling in advanced silicon materials and SOI devices. The materials and devices include heavily-doped SOI wafers, metal-bonded wafers, ultra-thin FD SOI MOSFETs and three-dimensional devices. All of them are promising solutions for "More Moore" and "Beyond Moore" applications. Their electrical properties have been analyzed by systematic electrical measurements, which are very informative for performance optimization. On the other hand, the transport models have been developed in order to extract material and device parameters. Ultimately, appropriate applications have been proposed based on these transport models.

Both experiments and simulations are used as the research methodologies in the electrical characterization and transport modeling. Several technical conclusions will be presented. Our study also opens the door for new innovations, which will be presented in the perspectives section.

Main conclusions

1. In chapter 2, we extended for the first time the pseudo-MOSFET technique to heavily-doped SOI wafers (10^{19} ~ 10^{20} cm^{-3}). Unusual pseudo-MOSFET characteristics were obtained, indicating two mechanisms: surface accumulation and volume conduction. Adapted models for both mechanisms were proposed for parameters extraction. The extracted parameters were validated by SIMS, Hall effect and four-point probe measurements. We showed that pseudo-MOSFET can independently provide both the carrier concentration and mobility (in volume and at the interface) and it is much simpler than Hall effect measurements.

2. In chapter 3, we demonstrated by experiments and simulations that the Schottky diode (formed by the probe and silicon) governs the current-voltage behavior of metal-bonded wafers. The Schottky diode is modulated by a series resistance, which permits estimating the quality of bonding interface before the metal-bonded wafers are used for 3D integration. Compared with other methods such as imaging and Kelvin cross, this estimation method is simpler, less destructive and does not need sophisticated fabrication steps.

3. In chapter 4, we investigated the parasitic bipolar effect in ultra-thin FD SOI MOSFETs (T_{si} > 5 nm). By TCAD simulations, we proved that band-to-band

tunneling was the main source for base current. We revisited all of the conventional methods to extract bipolar gain and only the comparison of drain leakage current between short- and long-channel transistors worked convincingly.

In addition, we found that a negative back-gate bias could efficiently suppress the parasitic bipolar effect in FD SOI MOSFETs. TCAD simulations showed that the parasitic bipolar effect was inhibited mainly by the increase of barrier height at body-source junction. Based on this effect, we proposed a new method to extract the bipolar gain, the value of which coincides well with the previous method. This new method using a single device is simple and advantageous.

4. Chapter 5 deals with coupling effects in multiple gate structures: inversion-mode and junctionless SOI FinFETs. We showed the experimental evidence of the coupling effect between front- and back-gates in the inversion-mode double-gate SOI FinFETs. A 2D potential model was developed and also adapted to full depletion region of junctionless SOI FinFETs. This analytical model considers 2D coupling effects and can quickly predict the effect of coupling on the threshold voltage, as a function of device geometry

   We proposed a compact model of the carrier density for single-, double-gate and triple-gate junctionless transistors. TCAD simulations verified its pertinence in the partial depletion region. Based on this simple model, the threshold voltage and maximum body size enabling full depletion can easily be determined. These two properties are useful for optimizing the switch-off characteristics of junctionless transistors.

   Most parameters extraction methods based on $I_D(V_{FG})$ curves in literature do not work in accumulation mode of nano-channel JL SOI FinFETs due to strong coupling effect. Nevertheless, TCAD simulations revealed a “weak” accumulation region ($V_{FG}-V_{FBF} < 0.2$ V for $N_D \sim 10^{19}$ cm^{-3}), where the coupling effect can be neglected. That region allows the extraction of flat-band voltage, low-field mobility and doping concentration in the nano-channel JL SOI FinFETs.

   These methods for JL SOI FinFETs were successfully applied to the experimental result in heavily-doped GaN JL FinFETs. The extracted doping concentration coincided well with the one obtained from Hall effect measurements. Combining

the extracted flat-band voltage and doping concentration, we determined the threshold voltage from the 2D potential model and carrier profile model. Our extraction procedure provides a fast and simple solution for electrical characterization in any heavily-doped MOS structures.

Further perspectives

Our study opened new questions and directions for further improvements in this research field.

1. For substrate characterization, we used pseudo-MOSFET for doped SOI and adapted current measurements for metal-bonded wafers. The use of pseudo-MOSFET should be extended to other materials, such as III-V compounds. The models discussed here were proposed for silicon, but they are usable for other materials. Our measurement technique accompanied by the models can deliever important information about dopant activation in heavily doped SOI films. For metal-bonded structures, we modeled them as a Schottky barrier due to the probe, modulated by the series resistance linked to the bonding quality. Different kinds of metals could be used for bonding and our access strategy should still stay available.
2. At the device level, we studied the parasitic bipolar effect in double-gate SOI MOSFETs. The leakage enhanced by parasitic bipolar effect has been evidenced, but its effect on the ICs is even more important. Therefore, compact models such as SPICE are needed to include the effect of parasitic bipolar effect on the leakage in ICs. The parasitic bipolar effect in triple-gate SOI transistors should be investigated.
3. When working with multiple-gate devices, the difficulty for the modeling and parameters extraction comes from the coupling effects. The potential and carrier profile models for junctionless SOI FinFETs, only validated by TCAD simulations, are short of experimental verifications.

My smart younger colleagues will complete this work and find the keys of these doors presented in future perspectives. I thank them in advance.

Abstract/Résumé

Title: Electrical characterization and modeling of advanced SOI materials and devices

This thesis is dedicated to the electrical characterization and transport modeling in advanced SOI materials and devices for ultimate micro-nano-electronics. SOI technology is an efficient solution to the technical challenges facing further downscaling and integration. Our goal was to develop appropriate characterization methods and determine the key parameters. Firstly, the conventional pseudo-MOSFET characterization was extended to heavily-doped SOI wafers and an adapted model for parameters extraction was proposed. We developed a nondestructive electrical method to estimate the quality of bonding interface in metal-bonded wafers for 3D integration. In ultra-thin fully-depleted SOI MOSFETs, we evidenced the parasitic bipolar effect induced by band-to-band tunneling, and proposed new methods to extract the bipolar gain. We investigated multiple-gate transistors by focusing on the coupling effect in inversion-mode vertical double-gate SOI FinFETs. An analytical model was proposed and subsequently adapted to the full depletion region of junctionless SOI FinFETs. We also proposed a compact model of carrier profile and adequate parameter extraction techniques for junctionless nanowires.

Keywords: Silicon-on-Insulator, pseudo-MOSFET, heavily-doped SOI, metal-bonded wafers, parasitic bipolar effect, band-to-band tunneling, back-gate, bipolar gain, coupling effect, inversion-mode SOI FinFETs, junctionless SOI FinFETs

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Titre: Caractérisation électrique et modélisation du transport dans matériaux et dispositifs SOI avancés

Cette thèse est consacrée à la caractérisation et la modélisation du transport électronique dans des matériaux et dispositifs SOI avancés pour la microélectronique. Tous les matériaux innovants étudiés (ex: SOI fortement dopé, plaques obtenues par collage *etc.*) et les dispositifs SOI sont des solutions possibles aux défis technologiques liés à la réduction de taille et à l'intégration. Dans ce contexte, l'extraction des paramètres électriques clés, comme la mobilité, la tension de seuil et les courants de fuite est importante. Tout d'abord, la caractérisation classique pseudo-MOSFET a été étendue aux plaques SOI fortement dopées et un modèle adapté pour l'extraction de paramètres a été proposé. Nous avons également développé une méthode électrique pour estimer la qualité de l'interface de collage pour des plaquettes métalliques. Nous avons montré l'effet bipolaire parasite dans des MOSFET SOI totalement désertés. Il est induit par l'effet tunnel bande-à-bande et peut être entièrement supprimé par une polarisation arrière. Sur cette base, une nouvelle méthode a été développée pour extraire le gain bipolaire. Enfin, nous avons étudié l'effet de couplage dans le FinFET SOI double grille, en mode d'inversion. Un modèle analytique a été proposé et a été ensuite adapté aux FinFETs sans jonction (junctionless). Nous avons mis au point un modèle compact pour le profil des porteurs et des techniques d'extraction de paramètres.

Mots-clefs: Silicium sur Isolant, pseudo-MOSFET, SOI fortement dopé, collage métallique des plaques, effet bipolaire parasite, effet tunnel bande-à-bande, grille arrière, gain bipolaire, effets de couplage, SOI FinFET, SOI FinFET sans jonctions

Publications

Journal Papers

1. **F. Y. Liu**, I. Ionica, M. Bawedin and S. Cristoloveanu, "Parasitic bipolar effect in ultra-thin FD SOI MOSFETs," *Solid-State Electronics*, 2015.
2. **F. Y. Liu**, I. Ionica, M. Bawedin and S. Cristoloveanu, "Extraction of the Parasitic Bipolar Gain Using the Back-gate in Ultra-thin FD SOI MOSFETs," *IEEE Elec. Dev. Lett.*, vol. 32, no. 2, pp. 96~98, 2015.
3. S-J. Chang, M. Bawedin, Y. F. Guo, **F. Y. Liu**, K. Akarvardar, J-H. Lee, J-H. Lee, I. Ionica and S. Cristoloveanu, "Enhanced coupling effects in vertical double-gate FinFETs," *Solid-State Electronics*, vol. 97, pp. 88~98, 2014.
4. **F. Y. Liu**, A. Diab, I. Ionica, K. Akarvardar, C. Hobbs, T. Ouisse, X. Mescot and S. Cristoloveanu, "Characterization of Heavily Doped SOI wafers under Pseudo-MOSFETs Configuration," *Solid-State Electronics*, vol. 90, pp.65~72, 2013.

Conference Papers

1. M. S. Parihar, **F. Y. Liu,** C. Navarroa, S. Barraud, M. Bawedin, I. Ionica, A. Kranti and S. Cristoloveanu, "Back-gate effects and detailed characterization of junctionless transistor," ESSDERC 2015, accepted.
2. **F. Y. Liu**, I. Ionica, M. Bawedin and S. Cristoloveanu, "A simple compact model for carrier distribution and its application in single-, double- and triple-gate junctionless transistors," *Proceedings of EuroSOI & ULIS*, Bologna, Italy, 2015.
3. **F. Y. Liu**, I. Ionica, M. Bawedin and S. Cristoloveanu, "Effect of back-gate on parasitic bipolar effect in FD SOI MOSFETs," *Proceedings of IEEE S3S Conference*, San Francisco, USA, 2014, pp. 85~86.
4. **F. Y. Liu**, I. Ionica, M. Bawedin and S. Cristoloveanu, "Parasitic bipolar effect in advanced FD SOI MOSFETs: experimental evidence and gain extraction," *Proceedings of EuroSOI 2014*, Tarragona, Spain, 2014.
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6. Y. F. Guo, **F. Y. Liu**, S. J. Chang, J. F. Yao and S. Cristoloveanu, "An analytical model of back-gate coupling effects in vertical double-gate SOI MOSFETs," *Proceeding of EuroSOI 2013*, Paris, France, 2013.
7. **F. Y. Liu**, A. Diab, I. Ionica, K. Akarvardar, C. Hobbs, T. Ouisse, X. Mescot and S. Cristoloveanu, "Transport Properties in Heavily Doped SOI Wafers," *Proceeding of EuroSOI 2012*, Montpellier, France, 2012.
8. S. Cristoloveanu, I. Ionica, A. Diab and **F. Y. Liu**, "The Pseudo-MOSFET : principles and recent trends," (invited), *12th Int. Symposium on High Purity Silicon, 222nd Meeting of the Electrochemical Soc.,* Honolulu, Hawaii, USA, 2012.
9. C. Q. Xu, P. Batude, B. Sklenard, M. Vinet, M. Mouis, B. Previtali, **F. Y. Liu**, J. Guerrero, K. Yckache, P. Rivallin, V. Mazzocchi, S. Cristoloveanu, O. Faynot and T. Poiroux, "FDSOI: A solution to suppress boron deactivation in low temperature processed devices," *12th IWJT*, Shanghai, 2012, pp. 69~72.

Résumé du travail de la thèse en français

Chapitre 1: Introduction générale

Cette thèse est consacrée à la caractérisation et la modélisation du transport électronique dans des matériaux et dispositifs SOI avancés pour la microélectronique. Tous les matériaux innovants étudiés (ex: SOI fortement dopé, plaques obtenues par collage *etc.*) et les dispositifs SOI sont des solutions possibles aux défis technologiques liés à la réduction de taille et à l'intégration. Dans ce contexte, l'extraction des paramètres électriques clés, comme la mobilité, la tension de seuil et les courants de fuite est primordiale.

Le chapitre d'introduction présente brièvement les avantages, les défis et les progrès récents dans le domaine des technologies SOI.

Chapitre 2: Caractérisation des plaques SOI fortement dopées en configuration pseudo-MOSFET

Dans ce chapitre, nous avons adapté la technique pseudo-MOSFET à des plaques SOI fortement dopées. Dans la configuration pseudo-MOSFET, le film de silicium représente le corps du transistor et l'oxyde enterré (BOX) sert d'isolant de grille. Le substrat est utilisé comme contact de grille et deux pointes métalliques avec pression contrôlée servent de source et drain. Pour des plaques SOI non dopées ou peu dopées, la tension de grille induit une couche d'accumulation ou d'inversion à l'interface film/BOX. Pour les plaques SOI fortement dopées, nous avons mis en évidence deux modes de conduction comme le montre la Figure 1 :

a) Conduction volumique et conduction par le canal à l'interface film/BOX (Figure 1a) ;

b) Conduction volumique variable liée à la désertion partielle du film avec V_G (Figure 1b).

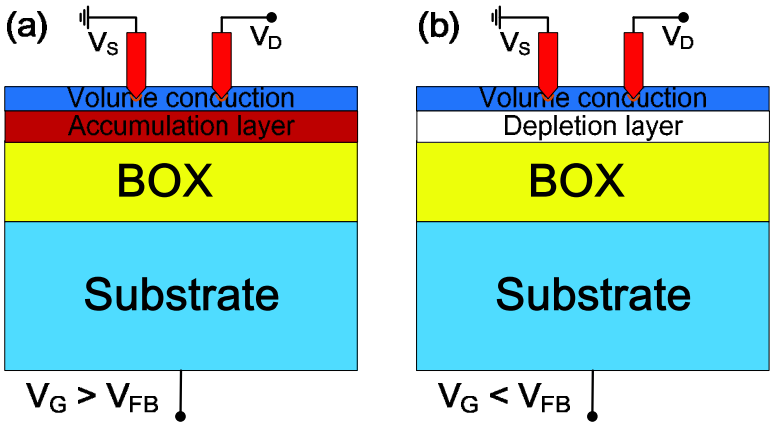

Figure 1 : *Régimes de conduction pour Ψ-MOSFET sur SOI très fortement dopé (exemple ici pour un dopage p avec du Bore). (a) Conduction en volume et par la couche d'accumulation; (b) conduction volumique variable.*

- **Conduction volumique variable**

La modélisation de ce régime s'appuie sur l'évaluation de la taille de la zone de charge d'espace. La largeur de cette zone de désertion (W_D) dans le film est contrôlée par V_G. En première approximation et pour un film de type p, la relation est :

$$W_D = \frac{C_{BOX}}{qN_A}\left(V_G - V_{FB}\right) \tag{1}$$

L'équation (1) montre que l'extension de la couche de désertion dépend linéairement de V_G. Par conséquent, l'épaisseur de la partie conductrice du film (T_{si}–W_D) diminue linéairement avec V_G. En supposant que la mobilité dans le volume du film est constante, le courant de drain varie comme une fonction linéaire de W_D :

$$I_D = I_{vol} = qf_G\mu_{p,vol}N_A(T_{si} - W_D)V_D \tag{2}$$

où $\mu_{p,vol}$ représente la mobilité des trous dans le volume. En substituant Eq. (1) dans Eq. (2), le courant de volume I_{vol} devient :

$$I_{vol} = -f_G\mu_{p,vol}C_{BOX}(V_G - V_0)V_D \tag{3}$$

où V_0 est une tension caractéristique donnée par :

$$V_0 = V_{FB} + \frac{qN_A}{C_{BOX}} T_{si} \tag{4}$$

V_0 représente une tension fictive qui conduirait à la désertion complète du film et qui est mesurée par extrapolation à courant nul dans la région linéaire des courbes $I_D(V_G)$. V_0 est très grand (> 150 V) parce que la désertion complète ne peut pas être effectivement atteinte en raison du très fort dopage. V_0 donne la concentration des dopants N_A en utilisant Eq. (4). La pente de Eq. (3) permet l'extraction de la mobilité volumique μ_{vol}. La Figure 2 montre l'application de notre modèle sur les courants mesurés avec des films de 40 nm et 10 nm d'épaisseur.

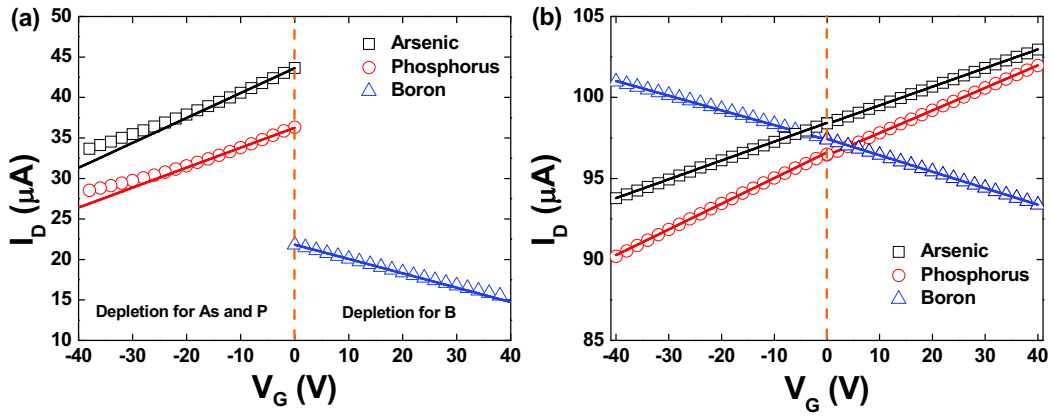

Figure 2 **:** *Courbes $I_D(V_G)$ expérimentales (symboles) et modélisées (lignes) dans le régime du conduction volumique pour (a) 40 nm et (b) 10 nm de film. SOI fortement dopé.*

- **Accumulation à l'interface film/BOX**

Lorsque la tension de grille V_G devient suffisamment élevée (positive pour des films de type n ou négative pour des films de type p), un canal d'accumulation peut se former à l'interface film/BOX (Figure 1a). En conséquence, le courant de drain comporte le courant de volume dans tout le film et le courant d'accumulation à l'interface film/BOX :

$$I_D = I_{vol} + I_{acc} \tag{5}$$

La Figure 3a montre le courant d'accumulation $I_{acc}(V_G)$.

Nous avons proposé une nouvelle fonction Y, Y_{acc}. Elle est dédiée exclusivement au canal d'accumulation et est définie comme :

$$Y_{acc} = \frac{I_D - I_{vol}}{\sqrt{g_m}} = \frac{I_{acc}}{\sqrt{g_m}} = \sqrt{f_G C_{BOX} V_D \mu_s}\,(V_G - V_{FB}) \qquad (6)$$

L'équation (6) annonce une variation linéaire de la courbe $Y_{acc}(V_G)$ (voir Figure 3b) Cette nouvelle fonction Y n'est applicable que pour le régime d'accumulation. La mobilité extraite de la pente de $Y_{acc}(V_G)$, est celle des porteurs majoritaires à l'interface film/BOX et peut être différente de la mobilité en volume μ_{vol} de l'équation (3).

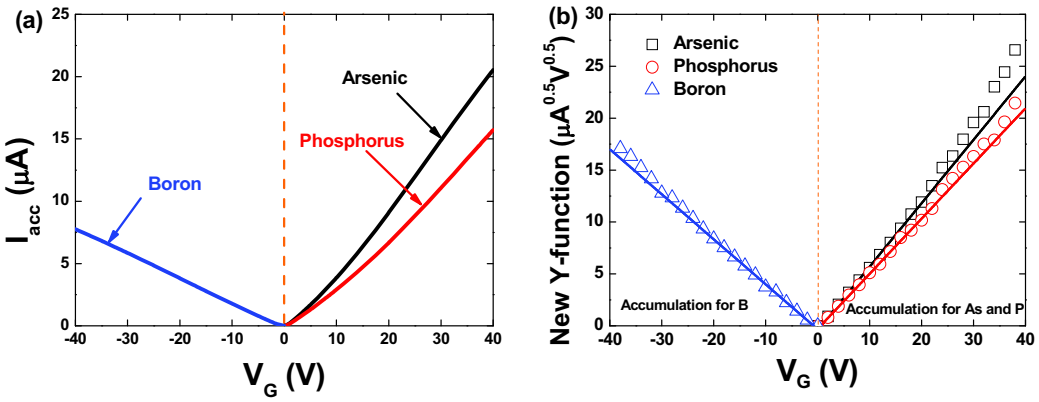

Figure 3 : *(a) $I_{acc}(V_G)$ et (b) fonction Y revisitée en fonction de la tension de grille pour le régime d'accumulation pour SOI fortement dopés avec 40 nm de film. Symboles: données expérimentales. Traits continues: approximation linéaire en utilisant l'équation (6).*

Les paramètres extraits à partir de nos modèles ont été validés par des expériences d'effet Hall, prouvant que le pseudo-MOSFET est parfaitement adapté à la caractérisation des SOI avec films très dopés.

Chapitre 3: Caractérisation des plaquettes réalisées par collage métallique

Ce chapitre est dédié à la caractérisation électrique de tranches de silicium métallisées et collées. En utilisant des simulations TCAD et des caractéristiques électriques expérimentales, la résistance liée à l'interface de collage est extraite. Cette méthode d'estimation est utile pour améliorer la qualité du collage. La configuration expérimentale, ainsi que les modèles équivalents pour des plaquettes vierges et collées, ont été fournis (Figure 4). Pour la plaquette vierge, deux contacts Schottky doivent être pris en compte: pointe/silicium (D_1) et silicium/chuck (D_2), comme indiqué dans Figure 4b. Nous avons prouvé que la jonction D_1 entre la pointe et le silicium régit le comportement de la tranche nue. De plus, nous avons démontré que cette même jonction est dominante également pour les plaques réalisées par collage.

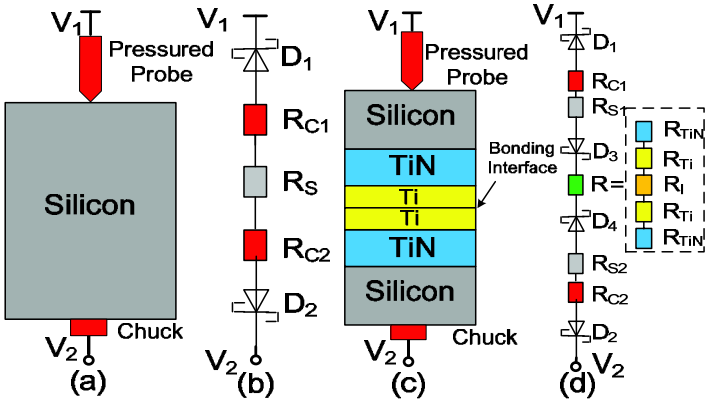

Figure 4 **:** *Configuration schématique de la mesure et modèle équivalent pour des plaquettes vierges (a, b) et collées (c, d). $D_{1,2,3,4}$ désignent les jonctions Schottky et $R_{C1,2}$ représentent les résistances de contact.*

La Figure 5 montre la caractéristique $I_P(V_P)$ pour les plaques collées avec des couches de liaison de Ti d'épaisseurs différentes : (a) avec 10 nm de Ti (appelées Bond10) et (b) avec 5 nm de Ti (appelés Bond5). Des plaques non recuites (RT) et recuites à 400°C de 2 heures ont été testées. Après recuit, le courant augmente, suggérant que le recuit diminue la résistance des contacts.

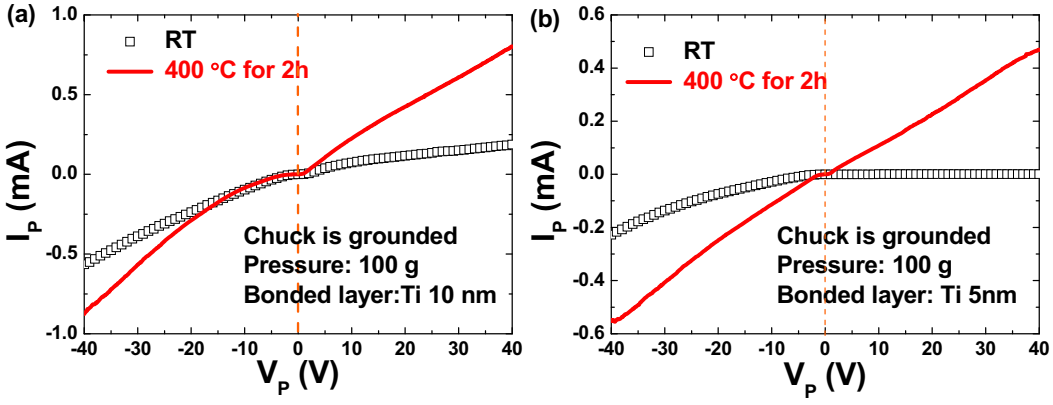

Figure 5 : *$I_P(V_P)$ Mesurée courbes des plaques collées avec différentes épaisseurs du film de Ti : (a) Bond10 et (b) Bond5.*

Nous avons modélisé nos courbes par la caractéristique d'une jonction Schottky (représentant le contact pointe/silicium) modulée par une résistance qui inclut toutes les résistances des matériaux et des interfaces (Figure 6a). La relation $I(V)$ d'une diode Schottky est exprimée par:

$$I = I_{Sat}\left(e^{qV/nkT} - 1\right) \tag{10}$$

$$I_{Sat} = A_{eff} A^* T^2 e^{-q\phi_B/kT} \tag{11}$$

où n est le facteur d'idéalité, A_{eff} est la surface effective, A^* est la constante de Richardson (~ 32) et Φ_B est la hauteur de barrière. Si $V >> 3kT/q$, la relation exponentielle domine et Eq. (10) peut être réécrite comme :

$$\log I = \log I_{Sat} + \frac{qV}{nKT \ln 10} \tag{12}$$

Le facteur d'idéalité n est obtenu à partir de la pente des courbes.

Pour les plaques collées, une résistance effective supplémentaire R_{eff} est introduite dans le modèle, afin d'estimer la qualité de l'interface de collage. Pour de grandes tensions $|V_P|$, la chute de tension aux bornes de la résistance série doit être prise en compte, et le courant $I_{bondend}$ à travers la plaque collée s'écrit comme :

$$\log I_{bonded} = \log I_{Sat} + \frac{q(V - I_{bonded}R_{eff})}{nkT \ln 10} \tag{13}$$

Ainsi, en substituant Eq. (12) dans Eq. (13), nous avons :

$$R_{eff} = \frac{\log(\gamma)}{\alpha I_{bonded}} \tag{14}$$

où $\gamma = I_{bare}/I_{bonded}$ et $\alpha = q/nkTln10$. Eq. (14) montre une dépendance linéaire de log(γ) avec I_{bonded}. Figure 6b représente log(γ) en fonction de I_{bonded}, qui est effectivement linéaire. La pente donne la résistance effective. Le Tableau-I montre les valeurs de R_{eff} avant et après recuit. Après le recuit, R_{eff} diminue. Ceci est cohérent avec le fait que le recuit améliore la qualité de l'interface de collage et, par conséquent, réduit les résistances séries.

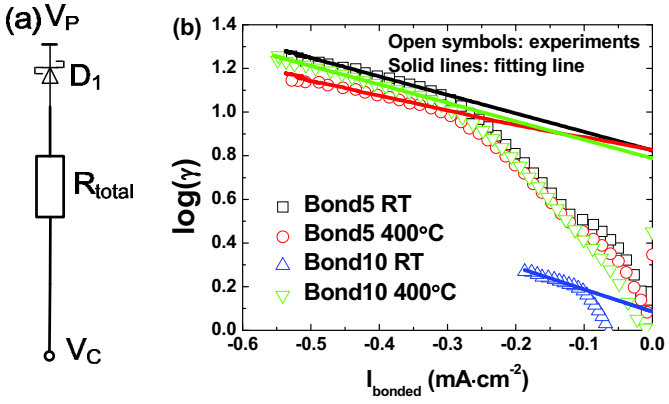

Figure 6 *: (a) Modèle simplifié pour les plaques collées et (b) log (γ) par rapport à I_{bonded} pour $|V_P|$ grandes.*

Tableau-I : *Paramètres extraits des expériences.*

			R_{eff} (kΩ)
Expériences	**Bond5**	**RT**	11
		400°C	6.3
	Bond10	**RT**	16
		400°C	10

Chapitre 4: Effet bipolaire parasite dans FD SOI MOSFET

Dans ce chapitre, nous nous concentrons sur les courants de fuites et l'impact du transistor bipolaire parasite (PBT) dans les dispositifs ultra-minces FD SOI (≤ 10 nm). Nous allons montrer, au travers d'expériences et simulations, qu'une amplification bipolaire est présente même dans les dispositifs à canaux courts ultra-minces.

4.1 Caractéristiques expérimentales

La Figure 7 compare les caractéristiques de transfert de dispositifs FD SOI à canal long (Figure 7a) et court (Figure 7b) sur 10 nm d'épaisseur de body. Dans les dispositifs longs, le courant de fuite (I_D pour V_{FG} < 0) augmente progressivement avec V_D. Pour un dispositif à canal court, le comportement est similaire mais uniquement à faible polarisation (0 < V_D < 1 V). Pour des tensions supérieures, l'augmentation des fuites avec V_D est plus rapide et dégrade les caractéristiques « OFF » du transistor. Afin de trouver une stratégie pour réduire ces fuites, nous avons besoin de comprendre l'origine de cette amplification soudaine se produisant à fort V_D dans les transistors courts.

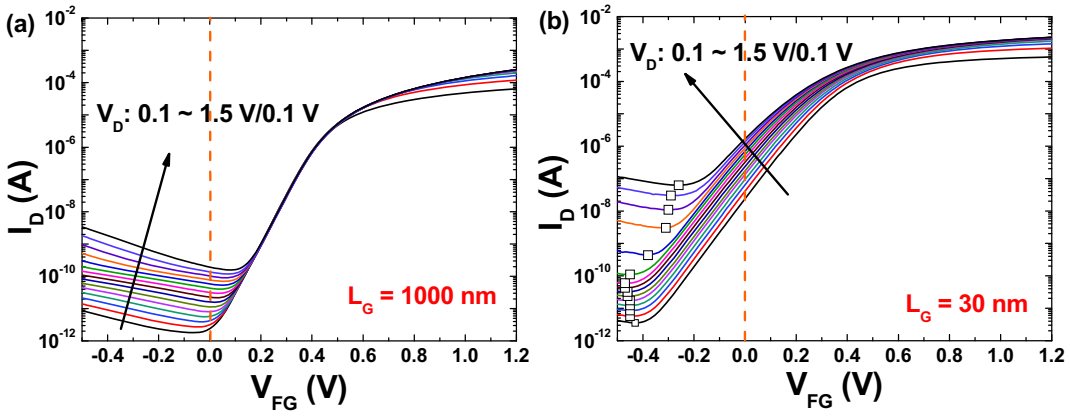

Figure 7 : *Courant de drain en fonction de la tension de grille dans des transistors NMOS FD SOI avec 10 nm d'épaisseur de film et différentes longueurs de canal : (a) L_G = 1µm et (b) L_G = 30 nm. T_{si} = 10 nm, W = 2µm et V_{BG} = 0 V.*

Les courants de drain, de source, de grille avant et arrière à V_{FG} = −0.5 V sont comparés pour un transistor canal long (Figure 8a) et pour un transistor canal court (Figure 8b) :

— Pour les dispositifs à canal long, le courant de source I_S reste faible lorsque V_D varie de 0.1 V à 1.5 V. Le courant de drain I_D est dominé par le courant de grille avant I_{FG}, ce qui explique la différence entre I_S et I_D. Le courant de grille arrière I_{BG} est d'abord l'équivalent de I_{FG} (V_D < 0.6 V), puis diminue (V_D > 0.6 V). L'ordre de grandeur pour I_{BG} est toujours inférieur à 10^{-10} A.

— Pour les dispositifs à canal court, I_{FG} ne domine la fuite que lorsque V_D < 1 V (Figure 8b); pour des valeurs de V_D supérieures, I_D et *Is* sont égaux et beaucoup plus grands que I_{FG}. Cette augmentation du courant de fuite révèle un mécanisme particulier apparaissant à fort V_D. Des simulations TCAD ont prouvé que l'amplification observée lorsque V_D augmente de 1 V à 1.5 V est induite principalement par l'effet tunnel bande à bande (BTBT). Cette amplification est associée à un effet bipolaire parasite (PBT).

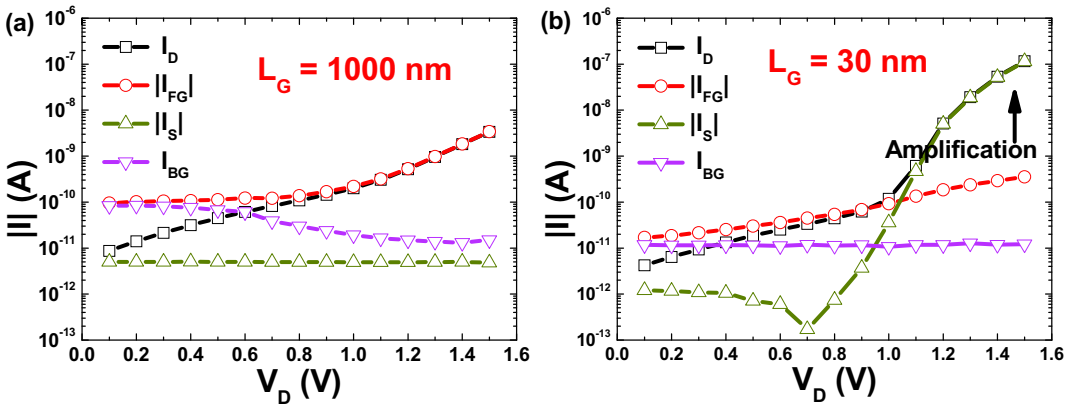

Figure 8 : *Comparaison des courants I_D, I_S, I_{FG} et I_{BG} à V_{FG} = -0.5 V pour deux transistors: (a) L_G = 1000 nm et (b) L_G = 30 nm.*

4.2 Suppression de l'effet bipolaire parasite

Afin de mettre en évidence l'effet de grille arrière sur l'effet bipolaire parasite, nous montrons dans Figure 9 les caractéristiques d'un transistor sur film mince (T_{si} = 10 nm). Pour les dispositifs avec L_G = 100 nm, le courant de fuite ne varie pas avec V_{BG} bien que la tension de seuil est décalée (Figure 9a). Un V_{BG} plus négatif peut réduire les fuites dans les dispositifs à canal court (L_G = 30 nm, Figure 9b) jusqu'à la valeur observée dans les dispositifs à canal long (quand il n'y a pas d'amplification). Pour V_{BG} encore plus négatif

(≤−3 V), le courant de fuite reste constant. Cette tendance indique qu'une tension de grille arrière négative dans les dispositifs courts est efficace pour atténuer le courant de fuite amplifié par le PBT latéral, et ceci jusqu'à sa totale suppression. Les simulations TCAD démontrent qu'une tension de grille arrière négative supprime l'effet bipolaire parasite principalement en augmentant la hauteur de barrière entre la jonction body-source ; la génération BTBT n'est pas affectée de manière significative par V_{BG}.

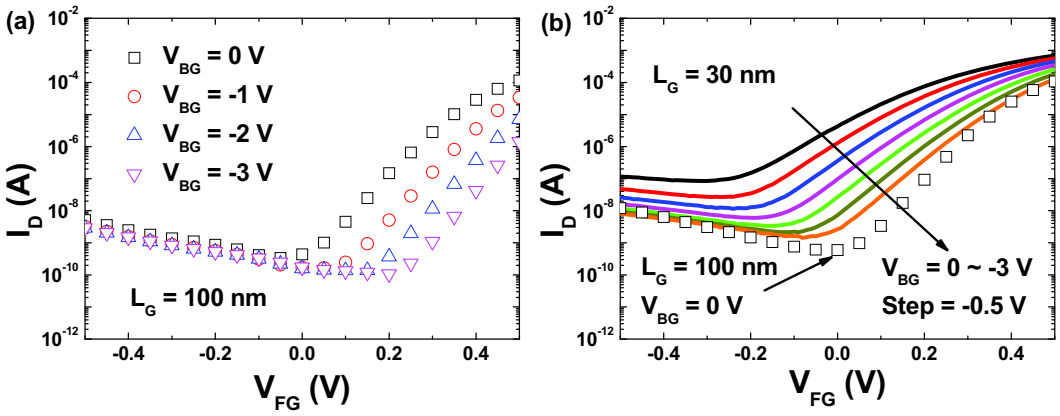

Figure 9: *Courants de drain pour des dispositifs avec body mince (T_{si} = 10 nm) en fonction de tension de grille avant, avec différents V_{BG}, pour (a) canal long et (b) canal court. V_D = 1.5 V.*

4.3 Extraction du gain bipolaire

L'effet PBT a été quantifié par l'évaluation du gain bipolaire, β. Plusieurs techniques existaient déjà pour son extraction dans les MOSFETs partiellement désertés mais s'avèrent inefficaces dans notre cas. Nous avons proposé deux méthodes pour extraire β dans les transistors complètement désertés :

— Comparaison des courants de fuite entre transistors à canal court et à canal long (méthode D).

— Comparaison des courants de fuite dans transistor à canal court sans V_{BG} et avec V_{BG} négatif (telle que l'effet bipolaire parasite est supprimé, méthode E).

Le gain bipolaire extrait par les deux méthodes est comparé dans Figure 10. Seule la région de faible injection pouvait être observée en raison du claquage de l'oxyde de grille aux V_D plus élevés. La Figure 10b, montrent que les deux méthodes d'extraction coïncident bien à faible injection.

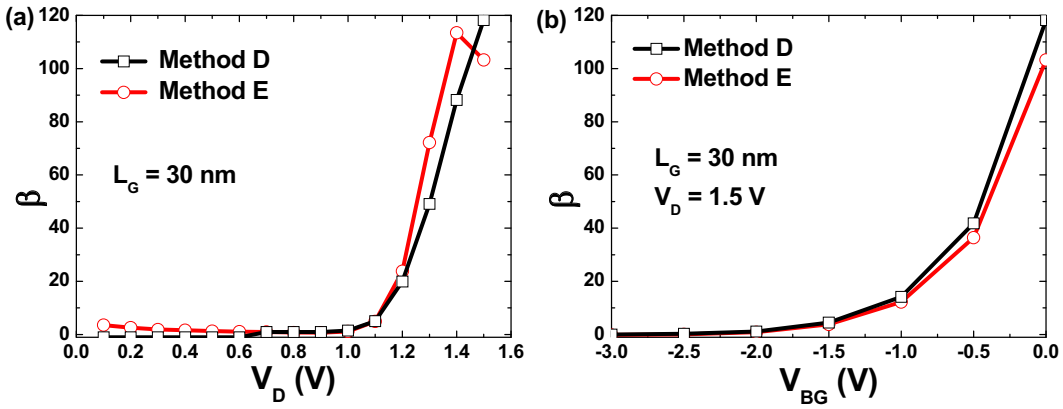

Figure 10 : *Le gain bipolaire en fonction des V_D (a) et de la tension de grille arrière (b) extrait à partir des données expérimentales avec les méthodes D et E.*

Chapitre 5: Effets de couplage tridimensionnel dans les dispositifs SOI

Dans ce chapitre, nous étudions systématiquement les effets de couplage 3D dans les dispositifs SOI dans différents régimes et architectures.

Partie A: Modélisation de potentiel et effets de couplage dans des transistors en inversion et dans des transistors sans jonction FinFET sur SOI

Nous avons étudié des FinFET double grille (DG) verticaux. La Figure 11 monte la section transversale d'un transistor. Il s'agit de transistors avec 3 grilles, mais l'oxyde du haut est suffisamment épais pour que son control électrostatique sur le canal soit négligeable. Nous proposons de décrire le potentiel *φ(x,y)* dans le body, comme étant parabolique :

$$\varphi(x,y) = a(y)x^2 + b(y)x + c(y) \qquad (12)$$

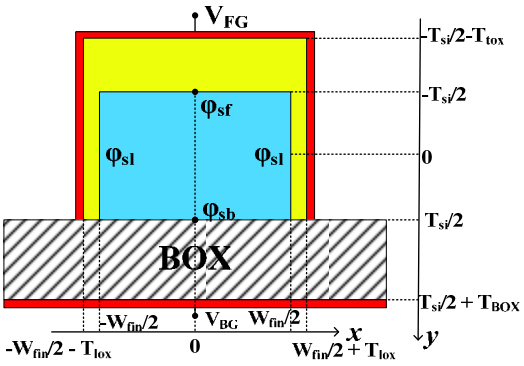

Figure 11 : *Section transversale du DG SOI FinFET vertical.*

En rajoutant les conditions aux limites, nous pouvons obtenir la distribution de potentiel 2D comme solution de l'Equation (12). La distribution 2D du potentiel est utile pour quantifier les tensions de seuil du canal avant/arrière (V_{THF}/V_{THB}). La comparaison de $V_{THF}(V_{BG})$ simulée et mesurée est indiquée dans Figure 12. Un accord global entre le modèle analytique et les résultats simulés peut être observé. Avec une interface arrière accumulée (V_{BG} < −20 V à Figure 12a), la tension de seuil du canal avant est constante. Pour V_{BG} plus grand, l'interface arrière est désertée et la tension de seuil pour la grille avant diminue linéairement avec V_{BG}, par couplage. La même tendance est observée pour $V_{THB}(V_{FG})$ (Figure 12b).

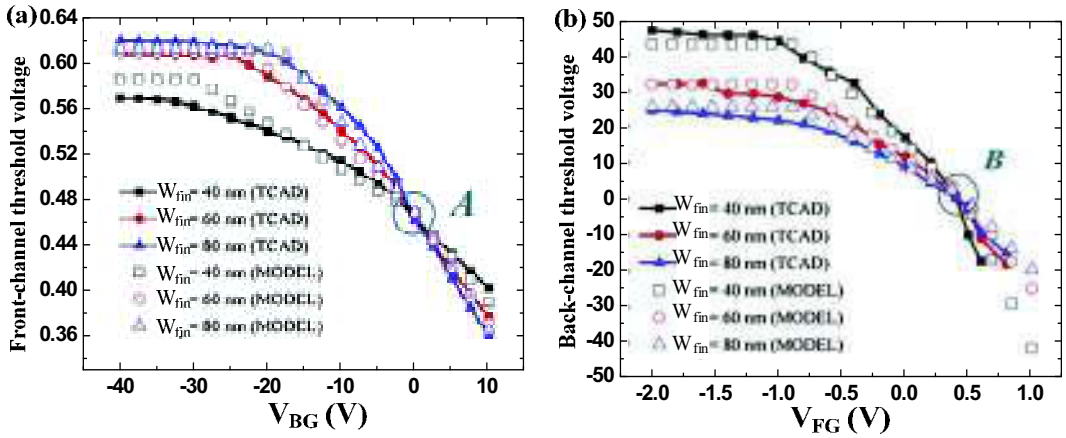

Figure 12 : *Effets de couplage pour FinFETs de largeur variable. (a) $V_{THF}(V_{BG})$; (b) $V_{THB}(V_{FG})$.*

Nous avons également étendu ce modèle pour le régime de désertion complète des FinFET sans jonctions (junction-less, JL). En raison du canal fortement dopé dans ces transistors sans jonctions, le potentiel satisfait l'équation de Poisson 2D :

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = -\frac{qN_D}{\varepsilon_{si}} \tag{13}$$

La tension de seuil calculée à partir de notre modèle coïncide avec celle extraite à partir de dg_m/dV_{FG} (Figure 13). L'écart pour un dispositif large (W_{fin} > 30 nm) peut éventuellement être attribué à l'effet des charges mobiles.

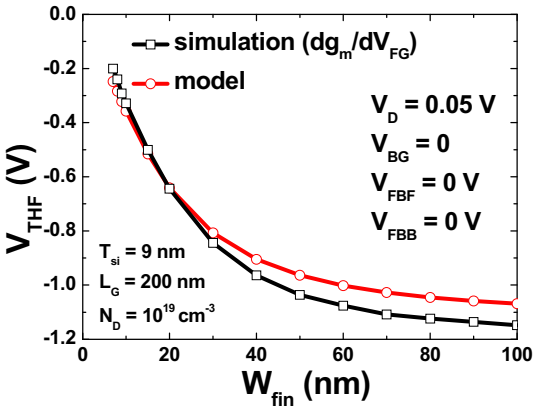

Figure 13 : *Tension de seuil de la grille avant en fonction de la largeur des transistors à partir de notre modèle et à partir du second pic de* dg_m/dV_{FG}.

Partie B: Modélisation de FinFET sans jonctions pour l'extraction de paramètres

Le profil de porteurs de charges majoritaires dans un transistor à grille unique présente une variation progressive dans la section transversale du canal. Cette variation est régie par la longueur de Debye et peut se modéliser comme :

$$N^*(y) = \frac{N_D}{2}\left(1 + tanh\left(\frac{y + T_{si}/2 - W_D}{\alpha L_D}\right)\right) \tag{14}$$

où L_D est la longueur de Debye ($L_D = \sqrt{\frac{\varepsilon_{si} kT}{q^2 N_D}}$) et α est un facteur correcteur ($\alpha \approx 1.7$), W_D est la largeur de la zone de charge d'espace due à la grille supérieure. La Figure 14 monte

la distribution de porteurs majoritaires à travers le canal d'un transistor sans jonctions, avec une seule grille, pour T_{si} = 50 nm (Figure 14a) et T_{si} = 9 nm (Figure 14b). Les courbes modélisées sont reproduites par simulation. Un léger désaccord se manifeste pour T_{si} = 9 nm, notamment proche de l'interface arrière.

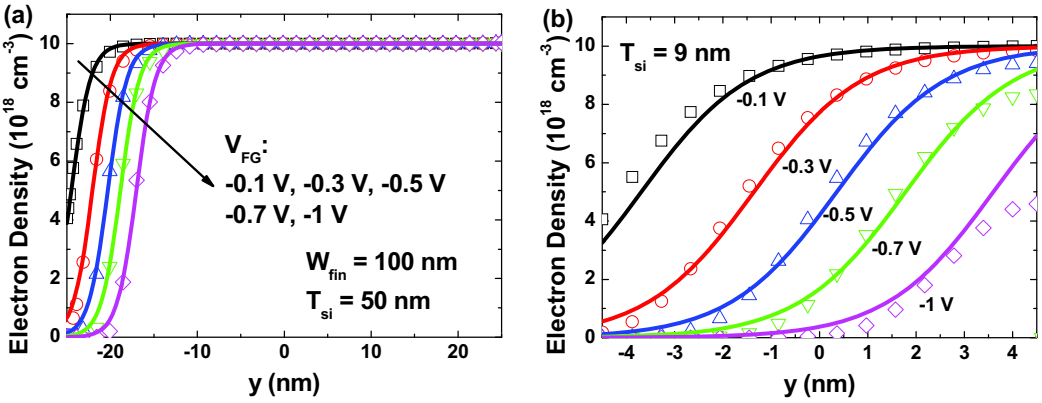

Figure 14 : *La comparaison modèle - simulations des profils de porteurs pour les transistors JL à grille unique avec $N_D = 10^{19}$ cm^{-3}: (a) T_{si} = 50 nm et (b) T_{si} = 9 nm. W_{fin} = 100 nm et L_G = 200 nm. V_{BG} = 0 V.*

- **Transistor JL double grille (DG)**

On considère un dispositif contrôlé par deux grilles latérales connectées ensemble à V_{FG}. Les deux régions de désertion s'élargissent quand V_{FG} baisse. Dans ce cas, nous supposons qu'une grille agit sur le dopage effectif défini par la grille opposée. Le profil dans ce cas va s'écrire comme :

$$N^*(x) = \frac{N_D}{4}\left(1+\tanh\left(\frac{x+W_{fin}/2-W_D}{\alpha L_D}\right)\right)\cdot\left(1+\tanh\left(\frac{-x+W_{fin}/2-W_D}{\alpha L_D}\right)\right) \quad (15)$$

Les profils des porteurs modélisés montrent un très bon accord avec les simulations 3D pour les dispositifs DG JL larges (Figure 15a). Dans les transistors DG JL plus étroits (Figure 15b), notre modèle montre un léger écart apparaissant au centre du canal quand la grille est polarisée sous le seuil.

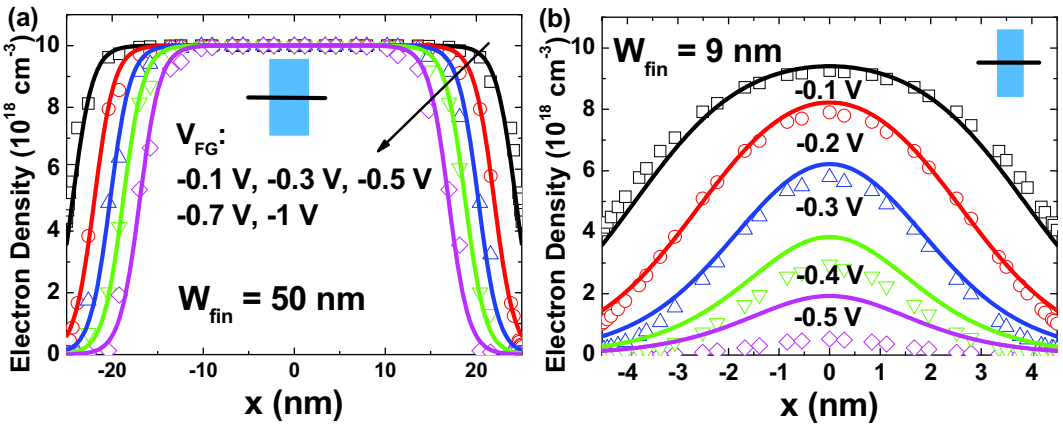

Figure 15 : *Comparaison des profils porteurs pour transistors JL DG avec $N_D = 10^{19}$ cm^{-3}: (a) W_{fin} = 50 nm (partiellement déserté) et (b) W_{fin} = 9 nm (entièrement déserté). T_{si} = 100 nm et L_G = 200 nm. V_D = 0.05 V et V_{BG} = 0 V. lignes solides = modèle analytique; symboles ouverts = simulations numériques.*

Basé sur notre modèle empirique du profil des porteurs dans le canal, nous avons déterminé la tension de seuil (Figure 16) et la taille maximale du body permettant la désertion complète du transistor (Figure 17).

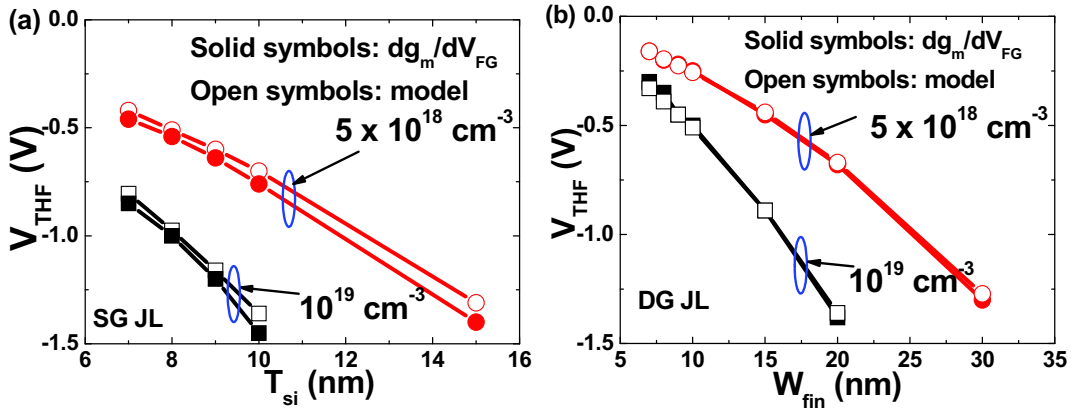

Figure 16 : *Comparaison des V_{THF} extraits avec notre méthode (symboles ouverts) et avec le pic de dg_m/dV_{FG} (symboles pleins) : (a) SG et (b) DG JL.*

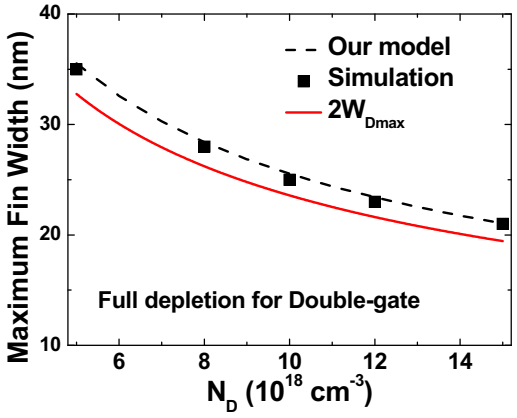

Figure 17 : *La taille maximale du body du transistor JL DG permettant la désertion complète du canal pour atteindre l'arrêt du transistor.*

Partie C: Extraction de paramètres dans des FinFET sans jonctions fabriqués en GaN

Les méthodes d'extraction de paramètres ont été testées sur des résultats expérimentaux pour des FinFETs en GaN fortement dopés. La concentration de dopage extraite est en accord avec les mesures par effet Hall. Les modèles proposés peuvent être utilisés pour l'analyse du couplage, pour la caractérisation et pour l'optimisation de la géométrie dans les FinFETs fortement dopés.

Chapitre 6: Conclusions générales et perspectives

Au cours de cette thèse, je me suis concentré sur la caractérisation et la modélisation du transport électrique dans les matériaux et dispositifs avancés sur SOI.

Tout d'abord, la caractérisation classique pseudo-MOSFET a été étendue aux plaques SOI fortement dopées et un modèle adapté pour l'extraction de paramètres a été proposé. Nous avons également développé une méthode électrique pour estimer la qualité de l'interface de collage pour des plaquettes métalliques. Nous avons montré l'effet bipolaire parasite dans des MOSFETs SOI totalement désertés induit par l'effet tunnel bande à bande. Cet effet parasite peut être entièrement supprimé par une polarisation arrière. Sur cette base, une nouvelle méthode a été développée pour extraire le gain bipolaire. Enfin, nous avons étudié l'effet de couplage dans le FinFET SOI double grille, en mode d'inversion. Un modèle analytique a été proposé et a été ensuite adapté aux FinFETs sans

jonction (junctionless). Nous avons mis au point un modèle compact pour le profil des porteurs et des techniques d'extraction de paramètres.

Plusieurs études intéressantes pourraient permettre d'aller plus loin:

- tester notre modèle pour évaluer la qualité du collage métallique sur d'autres matériaux,
- développer des modèles compacts pour l'effet parasite bipolaire,
- compléter la validation expérimentale de nos modèles de couplage pour les transistors multi-grille.

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